Features

- Meet ISO11898 Standard
- Support CAN FD and data rates up to 5 Mbps
- Typical Loop Delay: 110 ns
- 5 V power supply, 3.0 V ~ 5.5 V IO interface
- Receiver Common Mode Input Voltage: ±30 V
- Bus Fault Protection: ±42 V
- Up to 5 kV RMS Isolation Rating (WSOP16)
- 10 kV Surge Capability (WSOP16)
- ±100 kV/μs typ CMTI
- Junction Temperatures from −40°C to 150°C
- SOP8 and Wide-SOIC (WSOP8, WSOP16)
- BUS pin ESD Protection:
  - ±15 kV Human-Body Model
  - ±1.5 kV Charged-Device Model
- Safety-Related Certifications:
  - VDE Reinforced Insulation according to DIN VDE V 0884- 11: 2017-01
  - 3750 Vrms (SOP8) Isolation Rating per UL 1577
  - CSA C22.2 No. 62368- 1:19 3rd, IEC 62368- 1:2018 Ed. 3 and EN 62368- 1:2020
  - TUV Certification according to EN 60950- 1 and EN 61010- 1
  - CQC Certification per GB4943. 1-2011

Applications

- Industrial Automation
- Motor Control
- Solar Inverters
- Battery Charging and Management
- Power Meter
- Security Systems

Description

The AL1050 device is an isolated CAN transceiver which meets the ISO11898 High-speed CAN (Controller Area Network) physical layer standard. The device is designed to use in CAN FD networks up to 5 Mbps, and to enhance timing margin and higher data rates in long and high-loading networks. As the design, the device features cross-wire, overvoltage and loss of ground protection from −42 V to +42 V, overtemperature shutdown, a −30 V to +30 V common-mode range. The VCCA is the power supply input for RXD and TXD I/O pins which support 2.25V to 5.5V wide range. The 2nd power supply VCCB of CAN BUS side which support 4.5V to 5.5V range.

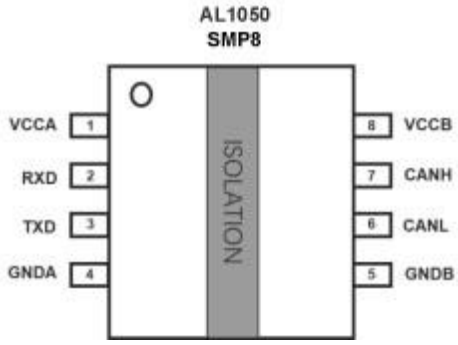
The devices integrate high-performance digital isolators with 5000 VRMS (WSOP16 packages) isolation ratings per UL 1577. These devices are also to be certified by VDE, UL, CSA, and CQC.

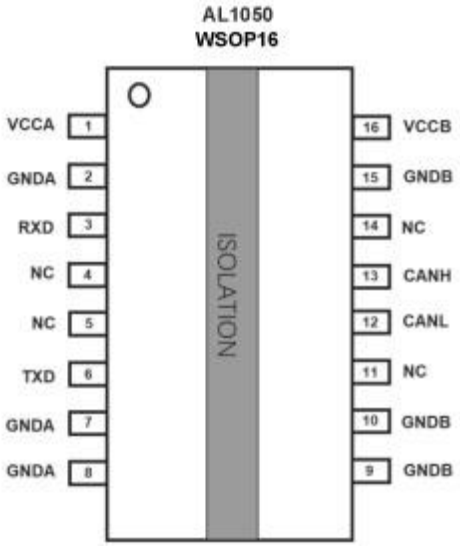
AL1050 is available in SOP8 and WSOP16 package, and is characterized from −40°C to +125°C.

Table of Contents

Features **1**
Applications **1**
Description **1**
Pin Configuration and Functions-AL1050 ..... **3**
Pin Functions 3
Specifications **4**
Absolute Maximum Ratings(1) 4
ESD, Electrostatic Discharge Protection 4
Recommended Operating Conditions 4
Thermal Information 4
Insulation Specifications 5
Electrical Characteristics 6
Electrical Characteristics- DC Specification 8
Switching Characteristics 9
Tape and Reel Information **10**
Package Outline Dimensions **12**
(WSOP8) 12
(WSOP16) 13
Order Information **14**

Pin Configuration and Functions-AL1050





Pin Functions

Pin			I/O	Description
Name	SMP8	WSOP16		
	AL1050	AL1050		
VCCA	1	1	–	Power supply, VCCA
RXD	2	3	O	Output, CAN receive data out
TXD	3	5	I	Input, CAN transmit data in
GNDA	4	2, 8	–	Ground connection for VCCA
GNDB	5	9, 10,15	–	Ground connection for VCCB
CANL	6	12	IO	Low level CAN bus input/output line
CANH	7	13	IO	High level CAN bus input/output line
VCCB	8	16	–	Power supply, VCCB
NC	–	4, 6, 7, 11, 14	–	No Connect

Specifications

Absolute Maximum Ratings (1)

Parameter		Min	Max	Unit
V_{CC}	Supply Voltage, V_{CCA}, V_{CCB} (2)	−0.5	6	V
V_{IO}	Voltage at IN1, IN2, OUT1, OUT2	−0.5	V_{CC} + 0.5	V
I_O	Output Current	−15	15	mA
T_J	Operating Virtual Junction Temperature		150	°C
T_{STG}	Storage Temperature Range	−65	150	°C

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

(2) This data was taken with the JEDEC low effective thermal conductivity test board.

(3) This data was taken with the JEDEC standard multilayer test boards.

ESD, Electrostatic Discharge Protection

Symbol	Parameter	Condition	Minimum Level	Unit
HBM	Human Body Model ESD, per ANSI/ESDA/JEDEC JS-001 (1)	Bus Pin	±15	kV
		All Pin Except Bus Pin	±6	kV
CDM	Charged Device Model ESD, per ANSI/ESDA/JEDEC JS-002 (2)	All Pin	±1.5	kV
LU	Latch Up, per JESD78	All Pin	±500	mA

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

Recommended Operating Conditions

Parameter		Min	Typ	Max	Unit
V_{CCB}	Supply voltage, V_{CCB}	4.5		5.5	V
V_{CCA}	Supply voltage, V_{CCA}	2.25		5.5	V
V_{IH}	High-level input voltage (data input)	2		V_{CC}	V
V_{IL}	Low-level input voltage (data input)	0		0.8	V
f_{data}	Data rate (1)	0		5	Mbps
T_A	Operating ambient temperature	−40	25	125	°C

(1) 5 Mbps is the maximum specified data rate, although higher data rates are possible.

Thermal Information

Package Type	θ_{JA}	θ_{JC}	Unit
8-Pin WSOP	85	43	°C/W
16-Pin WSOP	75	41	°C/W

Insulation Specifications

Symbol	Parameter	Conditions	VALUE		Unit
			WSOP8	WSOP16	
CLR	External clearance	Shortest terminal-to-terminal distance through air	> 7.6	> 7.6	mm
CPG	External creepage	Shortest terminal-to-terminal distance across the package surface	> 7.6	> 7.6	mm
DTI	Distance through the insulation	Minimum internal gap (internal clearance)	> 22	> 22	μm
DTC	Distance through the Molding compound	Minimum internal distance across the conductors inside the package	0.8	0.8	mm
CTI	Comparative tracking index		> 400	> 400	V
	Material group		I	I	
	Installation Classification	For Rated Mains Voltage ≤ 300 Vrms	I-III	I-III	
	Pollution degree		2	2	
C_{IO}	Isolation capacitance	V_{IO} = 0.4 × sin (2πft), f = 1 MHz	~ 0.5	~ 0.5	pF
R_{IO}	Isolation resistance	V_{IO} = 500 V	> 10^9	> 10^9	Ω
Isolation voltage(1)					
V_{IORM}	Maximum repetitive isolation voltage	AC voltage	1414	1414	V_{PK}
V_{IOWM}	Maximum working isolation voltage	AC voltage; TDDB Test	1000	1000	V_{RMS}
		DC voltage	1414	1414	V_{DC}
V_{IOTM}	Maximum transient isolation voltage	V_{TEST} = V_{IOTM}, t = 60 s (qualification); V_{TEST} = 1.2 x V_{IOTM}, t = 1 s (100% production)	7000	7000	V_{PK}
V_{IOSM}	Maximum surge isolation voltage	Test method per IEC 62368-1, 1.2/50 μs waveform, V_{TEST} = 1.6 × V_{IOSM} (qualification)	6000	6000	V_{PK}
q_{pd}	Apparent charge	Method a, After Input/Output safety test subgroup 2/3, V_{ini} = V_{IOTM}, tini = 60 s; $V_{pd(m)}$ = 1.2 × V_{IORM}, t_m = 10 s	≤5	≤5	pC
		Method a, After environmental tests subgroup 1, V_{ini} = V_{IOTM}, t_{ini} = 60 s; Vpd(m) = 1.6 × V_{IORM}, t_m = 10 s	≤5	≤5	
		Method b1; At routine test (100% production) and preconditioning (type test), V_{ini} = 1.2 x V_{IOTM}, t_{ini} = 1 s; Vpd(m) = 1.875 × V_{IORM}, t_m = 1 s	≤5	≤5	

(1) All pins on each side of the barrier tied together creating a two-terminal device.

Electrical Characteristics

All test conditions: V_{CCA} = 2.25 V ~ 5.5 V, V_{CCB} = 4.5 V ~ 5.5 V, T_A = −40°C to 125°C. Typical value is in V_{CCA} = 3.3 V, V_{CCB} = 5 V, T_A = +25°C.

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
Power Supply						
I_{CCA}	Supply current Side 1	Bus dominant, V_{CCA} = 2.25 V to 5.5 V, TXD = 0 V		2.3		mA
		Bus recessive, V_{CCA} = 2.25 V to 5.5 V, TXD = V_{CCA}		1.3		mA
		V_{CCA}=4.5 to 5.5V, TXD= 1Mbps 50% duty square wave		2.0		mA
		V_{CCA}=4.5 to 5.5V, TXD= 5Mbps 50% duty square wave		2.0		mA
I_{CCB}	Supply current Side 2	Bus dominant, TXD = 0 V, R_L = 60 Ω		50		mA
		Bus recessive, TXD = V_{CCA} , R_L = 60 Ω		6.0		mA
UV_{VCCA}	Rising under voltage detection, Side 1				2.25	V
UV_{VCCA}	Falling under voltage detection, Side 1		1.7			V
$V_{HYS(UVCC1)}$	Hysterisis voltage on V_{CCA} undervoltage lock-out (1)		75	150		mV
UV_{VCCB}	Rising under voltage detection, side 2			4.2	4.45	V
UV_{VCCB}	Falling under voltage detection, side 2		3.8	4.0	4.25	V
$V_{HYS(UVCC2)}$	Hysterisis voltage on V_{CCB} undervoltage lock-out (1)			200		mV
TXD Terminal						
V_{IH}	High level input voltage		0.7 × V_{CCA}			V
V_{IL}	Low level input voltage				0.3 × V_{CCA}	V
I_{IH}	High level input leakage current	TXD = V_{CCA}			1	uA
I_{IL}	Low level input leakage current	TXD = 0 V	−20			uA
C_I	Input capacitance (1)	V_{IN} = 0.4 x sin(2 x π x 1E+6 x t) + 2.5 V, V_{CCA} = 5 V		3		pF

(1). Parameters are provided by lab bench test and design simulation

Electrical Characteristics (Continued)

All test conditions: V_{CCA} = 2.25 V ~ 5.5 V, V_{CCB} = 4.5 V ~ 5.5 V, T_A = −40°C to 125°C. Typical value is in V_{CCA} = 3.3 V, V_{CCB} = 5 V, T_A = +25°C.

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
RXD Terminal						
$V_{OH} - V_{CCA}$	High level output voltage	I_O = −4 mA for 4.5 V ≤ V_{CCA} ≤ 5.5 V	−0.4			V
		I_O = −2 mA for 3.0 V ≤ V_{CCA} ≤ 3.6 V	−0.2			V
		I_O = −1 mA for 2.25 V ≤ V_{CCA} ≤ 2.75 V	−0.1			V
		I_O = −1 mA for 1.71 V ≤ V_{CCA} ≤ 1.89 V	−0.1			V
V_{OL}	Low level output voltage	I_O = 4 mA for 4.5 V ≤ V_{CCA} ≤ 5.5 V			0.4	V
		I_O = 2 mA for 3.0 V ≤ V_{CCA} ≤ 3.6 V			0.2	V
		I_O = 1 mA for 2.25 V ≤ V_{CCA} ≤ 2.75 V			0.1	V
		I_O = 1 mA for 1.71 V ≤ V_{CCA} ≤ 1.89 V			0.1	V
Driver Electrical Characteristics						
$V_{O(DOM)}$	Bus output voltage (Dominant), CANH	TXD = 0 V, 50 Ω ≤ R_L ≤ 65 Ω , C_L = open	2.75		4.5	V
	Bus output voltage (Dominant), CANL	TXD = 0 V, 50 Ω ≤ R_L ≤ 65 Ω , C_L = open	0.5		2.25	V
$V_{O(REC)}$	Bus output voltage (recessive), CANH and CANL	XD = V_{CCA} , R_L = open	2.0	0.5 x V_{CCB}	3.0	V

(1). Parameters are provided by lab bench test and design simulation

Electrical Characteristics-DC Specification

All test conditions: V_{CCA} = 2.25 V ~ 5.5 V, V_{CCB} = 4.5 V ~ 5.5 V, T_A = −40°C to 125°C. Typical value is in V_{CCA} = 3.3 V, V_{CCB} = 5 V, T_A = +25°C.

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
Power Supply						
$V_{OD(DOM)}$	Differential output voltage, CANH − CANL (dominant)	TXD = 0 V, 45 Ω ≤ R_L ≤ 50 Ω, C_L = open	1.4		3.0	V
		TXD = 0 V, 50 Ω ≤ R_L ≤ 65 Ω, C_L = open	1.5		3.0	V
		TXD = 0 V, R_L = 2240 Ω, C_L = open	1.5		5.0	V
$V_{OD(REC)}$	Differential output voltage, CANH-CANL (recessive)	TXD = V_{CCA}, R_L = 60 Ω, C_L = open				mV
		TXD = V_{CCA}, R_L = open, C_L = open				mV
V_{SYM_DC}	DC Output symmetry (V_{CCB} − $V_{O(CANH)}$ − $V_{O(CANL)}$)	R_L = 60 Ω, C_L = open, TXD = V_{CCA} or 0 V	−400		400	mV
$I_{SO(SS\_DOM)}$	Short circuit current steady state output current, dominant	V_{CANH} = −5 V to 40 V, CANL = open, TXD = 0 V	−100			mA
		V_{CANL} = −5 V to 40 V, CANH = open, TXD = 0 V			100	mA
$I_{SO(SS\_REC)}$	Short circuit current steady state output current, recessive	−30 V ≤ V_{BUS} ≤ 30 V, V_{BUS} = CANH = CANL, TXD = V_{CCA}	−5.0		5.0	mA
Receiver Electrical Characteristics						
V_{IT}	Differential input threshold voltage	|V_{CM}| ≤ 20 V	500		900	mV
		20 V ≤ |V_{CM}| ≤ 30 V	400		1000	
V_{HYS}	Hysteresis voltage for differential input threshold			120		mV
V_{CM}	Input common mode range		−30		30	V
$I_{OFF(LKG)}$	Power-off bus input leakage current	CANH = CANL = 5 V, V_{CCB} to GND via 0 Ω and 47 kΩ resistor			4.8	uA
C_I	Input capacitance to ground (CANH or CANL)	TXD = V_{CCA}		24.0	30	pF
C_{ID}	Differential input capacitance (CANH – CANL)	TXD = V_{CCA}		12.0	15	pF
R_{ID}	Differential input resistance	TXD = V_{CCA}; −30 V ≤ V_{CM} ≤ +30 V	30		80	kΩ
R_{IN}	Input resistance (CANH or CANL)	TXD = V_{CCA}; −30 V ≤ V_{CM} ≤ +30 V	15		40	kΩ
$R_{IN(M)}$	Input resistance matching: (1 − $R_{IN(CANH)}$/$R_{IN(CANL)}$) x 100% (1)	V_{CANH} = V_{CANL} = 5 V	−2.0		2.0	%
Thermal shutdown						
T_{TSD}	Thermal shutdown temperature (1)			170		°C
T_{TSD_HYST}	Thermal shutdown hysteresis (1)			5		°C

(1) Provided by bench test and design simulation

Switching Characteristics

All test conditions: V_{CCA} = 2.25 V ~ 5.5 V, V_{CCB} = 4.5 V ~ 5.5 V, T_A = −40°C to 125°C. Typical value is in V_{CCA} = 3.3 V, V_{CCB} = 5 V, T_A = +25°C.

Parameter		Conditions	Min	Typ	Max	Units
Switching Characteristics						
$t_{PROP(LOOP1)}$	Total loop delay, driver input TXD to receiver RXD, recessive to dominant	R_L = 60 Ω, C_L = 100 pF, $C_{L(RXD)}$ = 15 pF; input rise/fall time (10% to 90%) on TXD = 1 ns; 1.71 V ≤ V_{CCA} ≤ 1.89 V		125		ns
		R_L = 60 Ω, C_L = 100 pF, $C_{L(RXD)}$ = 15 pF; input rise/fall time (10% to 90%) on TXD =1 ns; 2.25 V ≤ V_{CCA} ≤ 5.5 V		122		ns
$t_{PROP(LOOP2)}$	Total loop delay, driver input TXD to receiver RXD, dominant to recessive	R_L = 60 Ω, C_L = 100 pF, $C_{L(RXD)}$ = 15 pF; input rise/fall time (10% to 90%) on TXD =1 ns; 1.71 V ≤ V_{CCA} ≤ 1.89 V		155		ns
		R_L = 60 Ω, C_L = 100 pF, $C_{L(RXD)}$ = 15 pF; input rise/fall time (10% to 90%) on TXD =1 ns; 2.25 V ≤ V_{CCA} ≤ 5.5 V		152		ns
$t_{UV\_RE\_ENABLE}$	Re-enable time after Undervoltage event	Time for device to return to normal operation from V_{CCA} or V_{CCB} under voltage event			300	µs
CMTI	Common mode transient immunity (1)	V_{CM} = 1200 V_{PK}		100		kV/µs
Driver Switching Characteristics						
t_{pHR}	Propagation delay time, HIGH TXD to driver recessive	R_L = 60 Ω and C_L = 100 pF; input rise/fall time (10% to 90%) on TXD = 1 ns		76		ns
t_{pLD}	Propagation delay time, LOW TXD to driver dominant			61		
$t_{sk(p)}$	Pulse skew (|t_{pHR} - t_{pLD}|)			14		
t_R	Differential output signal rise time (1)			45		
t_F	Differential output signal fall time (1)			45		
V_{SYM}	Output symmetry (dominant or recessive) ($V_{O(CANH)}$ + $V_{O(CANL)}$) / V_{CCB}	R_{TERM} = 60 Ω, C_{SPLIT} = 4.7 nF, C_L = open, R_L = open, TXD = 250 kHz, 1 MHz	0.9		1.1	V/V
t_{TXD_DTO}	Dominant time out	R_L = 60 Ω and C_L = open	1.2		3.8	ms

(1). Parameters are provided by lab bench test and design simulation

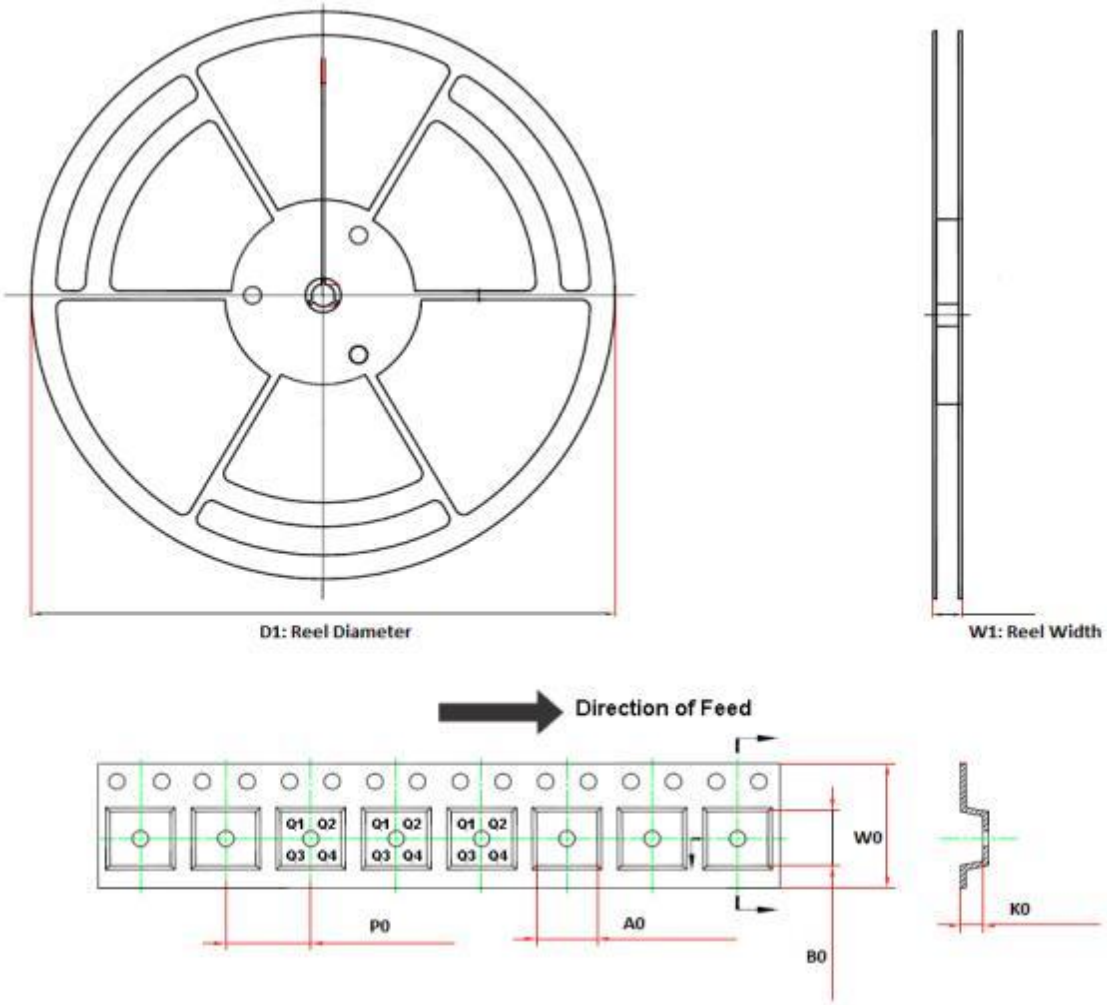
Switching Characteristics (Continued)

All test conditions: V_{CCA} = 2.25 V ~ 5.5 V, V_{CCB} = 4.5 V ~ 5.5 V, T_A = −40°C to 125°C. Typical value is in V_{CCA} = 3.3 V, V_{CCB} = 5 V, T_A = +25°C.

Parameter		Conditions	Min	Typ	Max	Units
Receiver Switching Characteristics						
t_{pRH}	Propagation delay time, bus recessive input to RXD high output	$C_{L(RXD)}$ = 15 pF		75		ns
t_{pDL}	Propagation delay time, bus dominant input to RXD low output			63		ns
t_R	Output signal rise time (RXD)			1.4		ns
t_F	Output signal fall time (RXD)			1.8		ns
CAN FD Timing parameters						
$t_{BIT(BUS)}$	Bit time on CAN bus output pins with $t_{BIT(TXD)}$ = 500 ns	R_L = 60 Ω, C_L = 100 pF, $C_{L(RXD)}$ = 15 pF; input rise/fall time (10% to 90%) on TXD =1 ns	435		530	ns
	Bit time on CAN bus output pins with $t_{BIT(TXD)}$ = 200 ns	R_L = 60 Ω, C_L = 100 pF, $C_{L(RXD)}$ = 15 pF; input rise/fall time (10% to 90%) on TXD =1 ns	155		210	ns
$t_{BIT(RXD)}$	Bit time on RXD output pins with $t_{BIT(TXD)}$ = 500 ns	R_L = 60 Ω, C_L = 100 pF, $C_{L(RXD)}$ = 15 pF; input rise/fall time (10% to 90%) on TXD =1 ns	400		550	ns
	Bit time on RXD output pins with $t_{BIT(TXD)}$ = 200 ns	R_L = 60 Ω, C_L = 100 pF, $C_{L(RXD)}$ = 15 pF; input rise/fall time (10% to 90%) on TXD =1 ns	120		220	ns
Δt_{REC}	Receiver timing symmetry with $t_{BIT(TXD)}$ = 500 ns	R_L = 60 Ω, C_L = 100 pF, $C_{L(RXD)}$ = 15 pF; input rise/fall time (10% to 90%) on TXD =1 ns; Δt_{REC} = $t_{BIT(RXD)}$ − $t_{BIT(BUS)}$	−65.0		40.0	ns
	Receiver timing symmetry with $t_{BIT(TXD)}$ = 200 ns	R_L = 60 Ω, C_L = 100 pF, $C_{L(RXD)}$ = 15 pF; input rise/fall time (10% to 90%) on TXD =1 ns; Δt_{REC} = $t_{BIT(RXD)}$ − $t_{BIT(BUS)}$	−45.0		15.0	ns

(1). Parameters are provided by lab bench test and design simulation

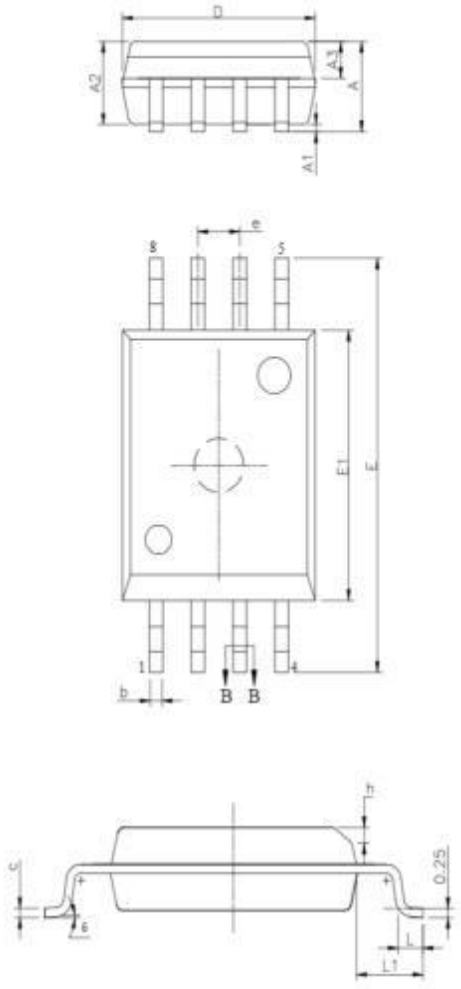
Tape and Reel Information



Order Number	Package	D1 (mm)	W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	W0 (mm)	Pin1 Quadrant
AL1050-SOP16	16-Pin WSOP	330.0	22.4	10.9	10.8	3	12	16	Q1

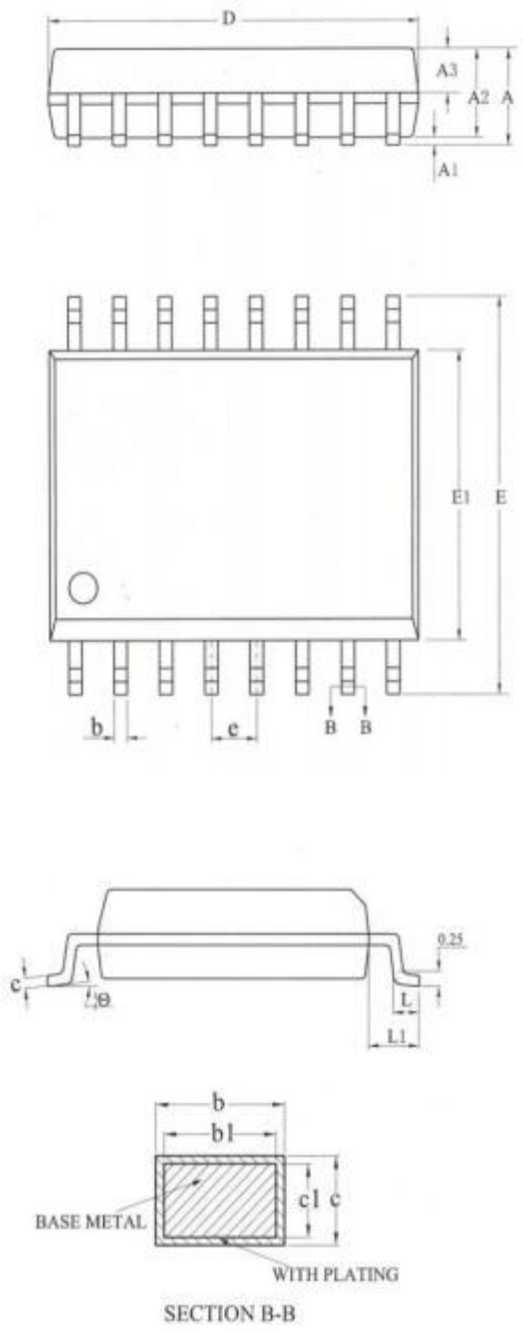
Package Outline Dimensions

(WSOP8)



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	—	—	2.65
A1	0.10	—	0.30
A2	2.25	2.30	2.35
A3	0.97	1.02	1.07
b	0.39	—	0.47
b1	0.38	0.41	0.44
c	0.25	—	0.29
c1	0.24	0.25	0.26
D	5.75	5.85	5.95
E	11.30	11.50	11.70
E1	7.40	7.50	7.60
e	1.27BSC		
h	0.25	—	0.50
L	0.50	—	1.00
L1	2.00REF		
θ	0	—	8°

(WSOP16)



SYMBOL	MILLIMETER			
	MIN	NOM	MAX	
A	—	—	2.65	
A1	0.10	—	0.30	1 3
A2	2.25	2.30	2.35	
A3	0.97	1.02	1.07	
b	0.35	—	0.44	
b1	0.34	0.37	0.39	
c	0.25	—	0.31	
c1	0.24	0.25	0.26	
D	10.10	10.30	10.50	
E	10.26	10.41	10.60	2
E1	7.30	7.50	7.70	
e	1.27BSC			
L	0.55	—	0.85	
L1	1.40BSC			
θ	0	—	8°	

Order Information

Order Number	Operating Temperature Range	Package	Marking Information	MSL	Transport Media, Quantity	Eco Plan
AL1050-SOP16	−40 to 125°C	16-Pin WSOP	AL1050	MSL3	Tape and Reel, 1500	Green

(1). Future product, contact ALONG factory for more information and sample

(2). Green: ALONG defines "Green" to mean RoHS compatible and free of halogen substances.