AL25WQ80

Ultra Low Power, 8M-bit

Serial Multi I/O Flash Memory Datasheet

Performance Highlight

- *Wide Supply Range from 1.65 to 3.6Vfor Read, Erase and Program*
- *Ultra Low Power consumption for Read, Erase andProgram*
- *X1, X2 andX4 Multi I/O Support*
- *High reliability with 100K cycling and 20 Year-retention*

Contents

1. Overview

1.1. General

- Single 1.65V to 3.60V supply
  - 1.65V-3.6V for Read, Erase and Program Operations
- Industrial Temperature Range -40C to 85C
- Serial Peripheral Interface (SPI) Compatible:
  - Mode 0 and Mode 3
- Single, Dual and Quad IO mode
  - 8M x 1 bit
  - 4M x 2 bits
  - 2M x 4 bits
- Flexible Architecture for Code and Data Storage
  - Uniform 256-byte Page Program
  - Uniform 256-byte Page Erase
  - Uniform 4K-byte Sector Erase
  - Uniform 32K/64K-byte Block Erase
  - Full Chip Erase

1.2. Performance

- Fast read
  - 4 I/O 104MHz with 2+4 dummy cycles， equivalent to416M
  - 2 I/O 104MHz with 4 dummy cycles， equivalent to208M
  - 1 I/O 104MHz with 8 dummy cycles
- Fast Program and Erase Speed
  - 2.5ms Page program time
  - 11ms Page erase time
  - 11ms 4K-byte sector erase time
  - 11ms 32K-byte block erase time
  - 11ms 64K-byte block erase time
- Burst read
  - 8/16/32/64 byte Wrap-Aroud
- Ultra Low Power Consumption
  - 0.5uA Deep Power Down current
  - 12uA Standby current
  - 4mA Active Read current at33MHz
  - 6mA Active Program or Erase current
- High Reliability
  - 100,000 Program / Erase Cycles
  - 20-year Data Retention

1.3. Software features

- One Time Programmable (OTP) Security Register
  - 3*512-Byte Security Registers With OTP Lock
- Software Protection Mode
  - The Block Protect (BP4, BP3, BP2, BP1, and BP0) bits define the section of the memory array that can be read but not change.
- 128 bit unique ID for each device
- Program/Erase Suspend and Program/Erase Resume
- JEDEC Standard Manufacturer and Device ID Read Methodology

1.4. Hardware features

- Hardware Protection Mode
  - Hardware Controlled Locking of Protected Sectors by WP Pin
- Industry Standard Green Package Options
  - 8-pin SOP (150mil/208mil)
  - 8-land USON (3x2x0.55mm)
  - 8-land WSON (6x5mm)
  - 8-pin TSSOP

2. Description

The AL25WQ80 is a serial interface Flash memory device designed for use in a wide variety of high-volume consumer based applications in which program code is shadowed from Flash memory into embedded or external RAM for execution. The flexible erase architecture of the device, with its page erase granularity it is ideal for data storage as well, eliminating the need for additional data storage devices.

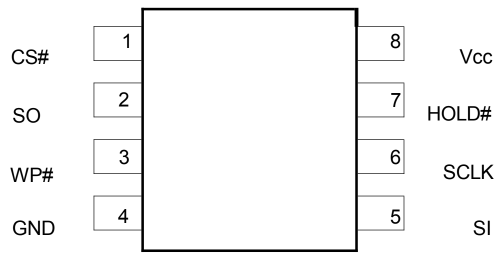
The erase block sizes of the device have been optimized to meet the needs of today's code and data storage applications. By optimizing the size of the erase blocks, the memory space can be used much more efficiently. Because certain code modules and data storage segments must reside by themselves in their own erase regions, the wasted and unused memory space that occurs with large sectored and large block erase Flash memory devices can be greatly reduced. This increased memory space efficiency allows additional code routines and data storage segments to be added while still maintaining the same overall device density.

The device also contains an additional 3*512-byte security registers with OTP lock (One-Time Programmable), can be used for purposes such as unique device serialization, system-level Electronic Serial Number (ESN) storage, locked key storage, etc.

Specifically designed for use in many different systems, the device supports read, program, and erase operations with a wide supply voltage range of 1.65V to 3.6V. No separate voltage is required for programming and erasing.

2.1. Pin Definition

Pin Configurations

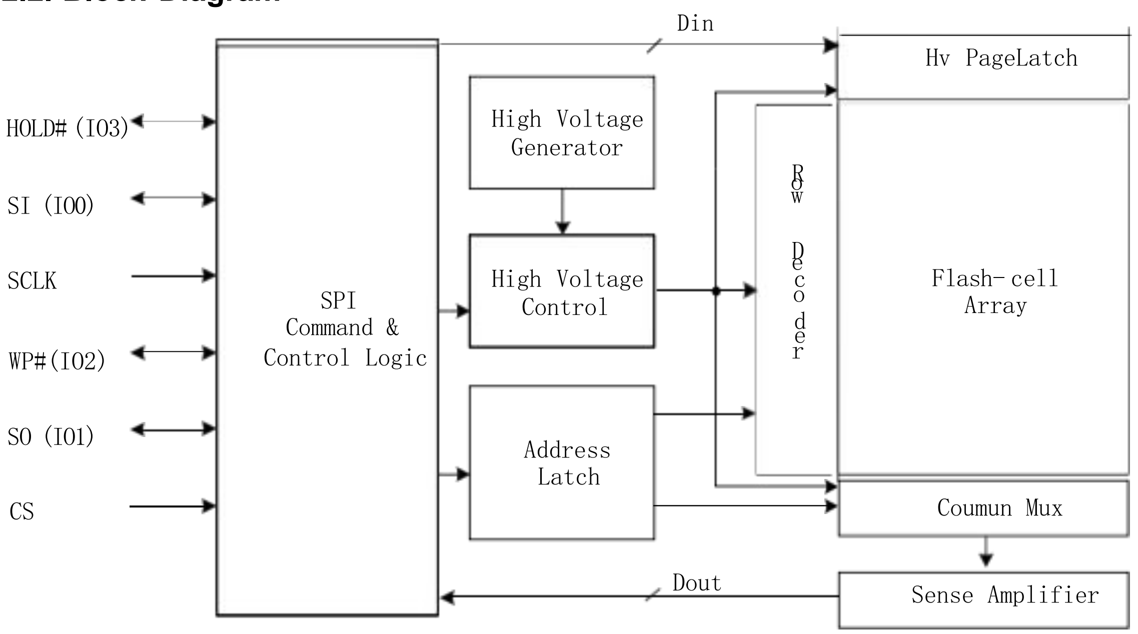


8-PIN SOP (150mil/200mil) andTSSOP

Pin Descriptions

No.	Symbol	Extension	Remarks
1	CS#		Chip select
2	SO	SIO1	Serial data output for 1 x I/O Serial data input and output for 4 x I/O read mode
3	WP#	SIO2	Write protection active low Serial data input and output for 4 x I/O read mode
4	GND	-	Ground of the device
5	SI	SIO0	Serial data input for 1x I/O Serial data input and output for 4 x I/O read mode
6	SCLK	-	Serial interface clock input
7	HOLD#	SIO3	To pause the device without deselecting the device Serial data input and output for 4 x I/O read mode
8	VCC	-	Power supply of the device

2.2. Block Diagram



2.3. Memory Address Mapping

The memory array can be erased in three levels of granularity including a full chip erase. The size of the erase blocks is optimized for both code and data storage applications, allowing both code and data segments to reside in their own erase regions.

AL25WQ80 Memory Organization

Block64K	Block32K	Sector	Address Range	
15	31 - 30	255	0FF000H	0FFFFFH
		……	……	……
		240	0F0000H	0F0FFFH
14	29 - 28	239	0EF000H	0EFFFFH
		……	……	……
		224	0E0000H	0E0FFFH
……	……	……	……	……
		……	……	……
		……	……	……
……	……	……	……	……
		……	……	……
		……	……	……
2	5 - 4	47	02F000H	02FFFFH
		……	……	……
		32	020000H	020FFFH
1	3 - 2	31	01F000H	01FFFFH
		……	……	……
		16	010000H	010FFFH
0	1 - 0	15	00F000H	00FFFFH
		……	……	……
		0	000000H	000FFFH

3. Electrical Specifications

3.1. Absolute Maximum Ratings

Parameters	Value
Storage Temperature	-65°C to +150°C
Operation Temperature	.-40°C to +125°C
Maximum Operation Voltage	4.0V
Voltage on Any Pin with respect to Ground	-0.6V to + 4.1V
DC Output Current	5.0 mA

NOTICE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Figure 3-1 Maximum Overshoot Waveform

Table 3-1 Pin Capacitance [1]

Symbol	Parameter	Max.	Units	Test Condition
C_{OUT}	Output Capacitance	8	pF	V_{OUT}=GND
C_{IN}	Input Capacitance	6	pF	V_{IN}=GND

Note:

Test Conditions: T_A = 25°C, F = 1MHz, Vcc = 3.0V.

Figure 3-2 Input Test Waveforms and Measurement Level

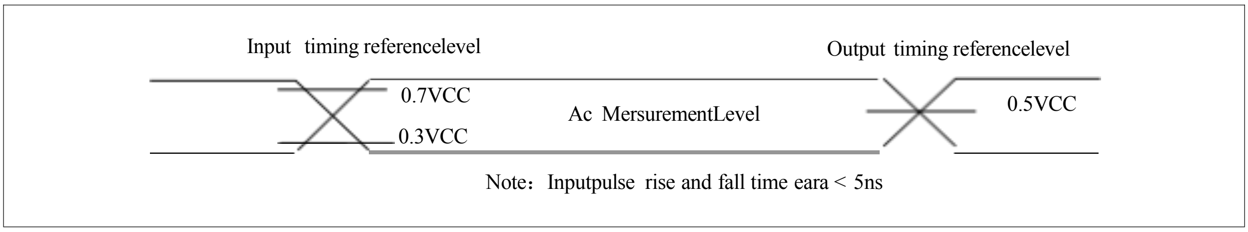
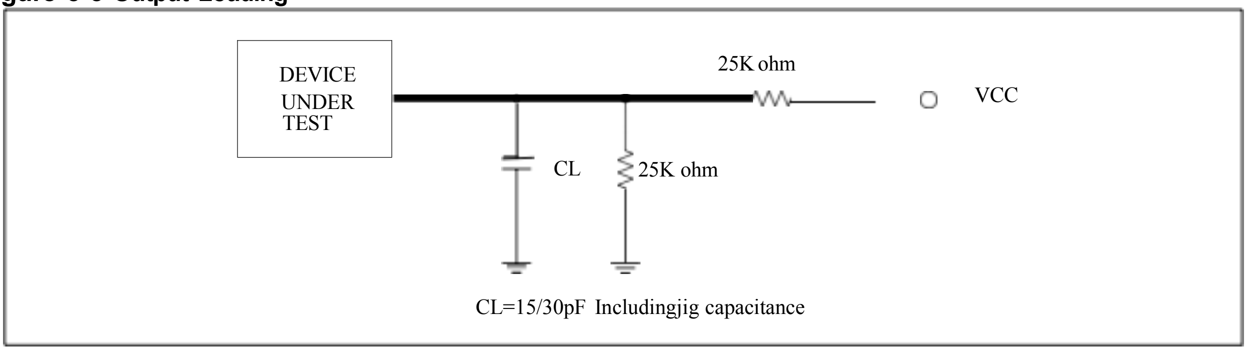


Figure 3-3 Output Loading



3.2. DC Characteristics

Table 3-2 DC parameters

Sym	Parameter	Conditions	1.65V to 2.3V			2 3V to 3 6V			Units
			Min.	Typ.	Max.	Min.	Typ.	Max.	
I_{DPD}	Deep power down current	CS#=Vcc, all other inputs at 0V or Vcc		0.5	1.5		0.5	1.5	uA
I_{SB}	Standby current	CS#, HOLD#, WP#=VIH all inputs at CMOS		12			12		uA
I_{CC1}	Low power read current (03h)	f=55MHz; IOUT=0mA		1.32	3.0		2.35	3.0	mA
I_{CC2}	Read current (0Bh)	f=85MHz; IOUT=0mA		1.85	4.0		2.82	4.0	mA
		f=104MHz; IOUT=0mA		-	-		2.82	4.5	mA
I_{CC3}	Program current	CS#=Vcc		2.6	6.0		5.1	6.0	mA
I_{CC4}	Erase current	CS#=Vcc		2.6	6.0		5.1	6.0	mA
I_{LI}	Input load current	All inputs at CMOS			1.0			1.0	uA
I_{LO}	Output leakage	All inputs at CMOS			1.0			1.0	uA
V_{IL}	Input low voltage				0.2Vcc			0.3Vcc	V
V_{IH}	Input high voltage		0.8Vcc			0.7Vcc			V
V_{OL}	Output low voltage	IOL=100uA			0.2			0.2	V
V_{OH}	Output high voltage	IOH=-100uA	Vcc-0.2			Vcc-0.2			V

Note

1. Typical values measured at 1.8V @ 25°C for the 1.65V to 3.6V range.
2. Typical values measured at 3.0V @ 25°C for the 2.3V to 3.6V range.

3.3. AC Characteristics

Symbol	Alt.	Parameter	1.65V~2.3V			2.3V~3 6V			Unit
			min		max	min	typ	max	
fSCLK	fC	Clock Frequency for the following instructions: FAST_READ, RDSFDP, PP, SE, BE32K, BE, CE, DP, RES,	D.C.		85			104	MHz
fRSCLK	fR	Clock Frequency for READ instructions			55			55	MHz
fTSCLK	fT	Clock Frequency for 2READ,DREAD instructions			85			104	MHz
	fQ	Clock Frequency for 4READ,QREAD instructions			85			104	MHz
fQPP		Clock Frequency for QPP (Quad page program)			85			104	MHz
tCH(1)	tCLH	Clock High Time	5.5			4.5			ns
tCL(1)	tCLL	Clock Low Time (fSCLK) 45% x (1fSCLK)	5.5			4.5			ns
tCLCH(7)		Clock Rise Time (peak to peak)	0.1			0.1			ns/v
tCHCL(7)		Clock Fall Time (peak to peak)	0.1			0.1			ns/v
tSLCH	tCSS	CS# Active Setup Time (relative to SCLK)	5			5			ns
tCHSL		CS# Not Active Hold Time (relative to SCLK)	5			5			ns
tDVCH	tDSU	Data In Setup Time	2			2			ns
tCHDX	tDH	Data In Hold Time	3			3			ns
tCHSH		CS# Active Hold Time (relative to SCLK)	5			5			ns
tSHCH		CS# Not Active Setup Time (relative to SCLK)	5			5			ns
tSHSL	tCSH	CS# Deselect Time From Read to next Read	15			15			ns
		CS# Deselect Time From Write,Erase,Program to Read Status Register	30			30			ns
tSHQZ(7)	tDIS	Output Disable Time			6			6	ns
tCLQV	tV	Clock Low to Output Valid Loading 30pF			7			7	ns
		Clock Low to Output Valid Loading 15pF			6			6	ns
tCLQX	tHO	Output Hold Time	0			0			ns
tHLCH		HOLD# Active Setup Time (relative to SCLK)	7			5			ns
tCHHH		HOLD# Active Hold Time (relative to SCLK)	5			5			ns
tHHCH		HOLD# Not Active Setup Time (relative to SCLK)	5			5			ns
tCHHL		HOLD# Not Active Hold Time (relative to SCLK)	5			5			ns
tHHQX	tLZ	HOLD# to Output Low-Z			6			6	ns
tHLQZ	tHZ	HOLD# to Output High-Z			6			6	ns
tWHSL(3)		Write Protect Setup Time	20			20			ns
tSHWL(3)		Write Protect Hold Time	100			100			ns
tDP		CS# High to Deep Power-down Mode			3			3	us
tRES1		CS# High To Standby Mode Without Electronic Signature Read			8			8	us
tRES2		CS# High To Standby Mode Without Electronic Signature Read			8			8	us
tW		Write Status Register Cycle Time		8	12		8	12	ms
tReady		Reset recovery time(for erase/program operation except WRSR)	70			70			us
		Reset recovery time(for WRSR operation)		8	12		8	12	ms

Table 3-3 AC parameters

3.4. AC Characteristics for Program and Erase

Table 3-4 AC parameters fro program and erase

Sym	Parameter	1.65V to 3.6V			Units
		Min.	Typ.	Max.	
$T_{ESL(6)}$	Erase Suspend Latency			30	us
$T_{PSL(6)}$	Program Suspend Latency			30	us
$T_{PRS(4)}$	Latency between Program Resume and next Suspend	0.3			us
$T_{ERS(5)}$	Latency between Erase Resume and next Suspend	0.3			us
t_{PP}	Page program time (up to 256 bytes)		2.5	3	ms
t_{PE}	Page erase time		11	12	ms
t_{SE}	Sector erase time		11	12	ms
t_{BE1}	Block erase time for 32K bytes		11	12	ms
t_{BE2}	Block erase time for 64K bytes		11	12	ms
t_{CE}	Chip erase time		11	12	ms

Note

1. tCH + tCL must be greater than or equal to 1/ Frequency.
2. Typical values givenfor TA=25°C. Not 100% tested.
3. Only applicable as a constraint for a WRSR instruction.
4. Program operation may be interrupted as often as system request. The minimum timing of tPRS must be observed before issuing the next program suspend command. However, in order for an Program operation to make progress, tPRS ≥ 100us must be included in resume-to-suspend loop(s). Not 100% tested.
5. Erase operation may be interrupted as often as system request. The minimum timing of tERS must be observed before issuing the next erase suspend command. However, in order for an Erase operation to make progress, tERS ≥ 200us must be included in resume-to-suspend loop(s). Notes. Not 100% tested.
6. Latency time is required to complete Erase/Program Suspend operation.
7. The value guaranteed by characterization, not 100% tested in production.

Figure 3-4 Serial Input Timing

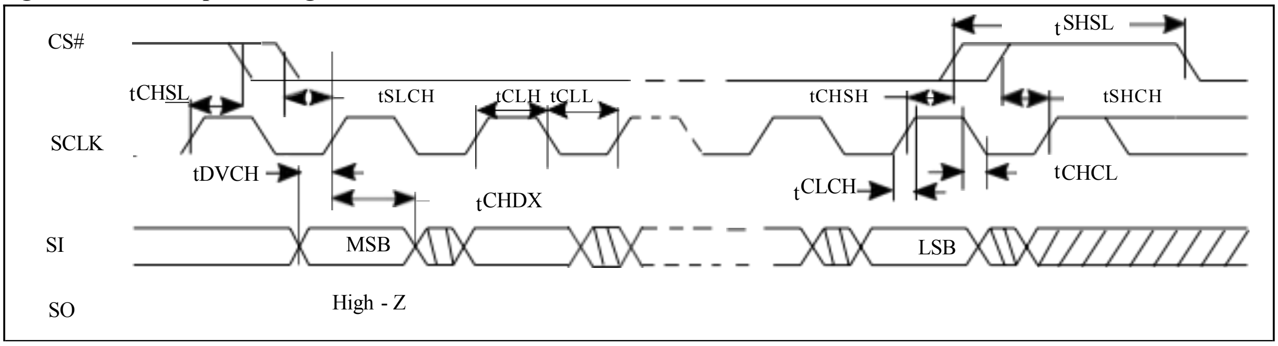


Figure 3-5 Output Timing

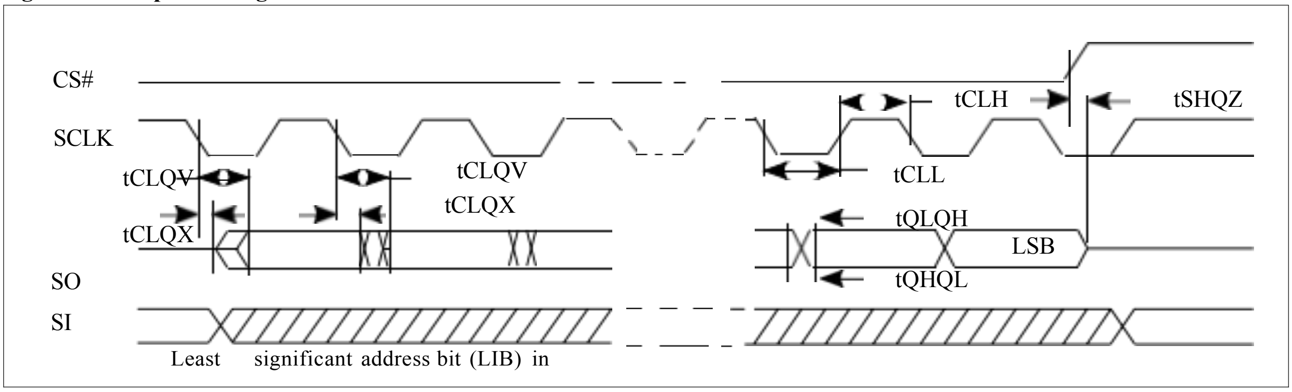


Figure 3-6 Hold Timing

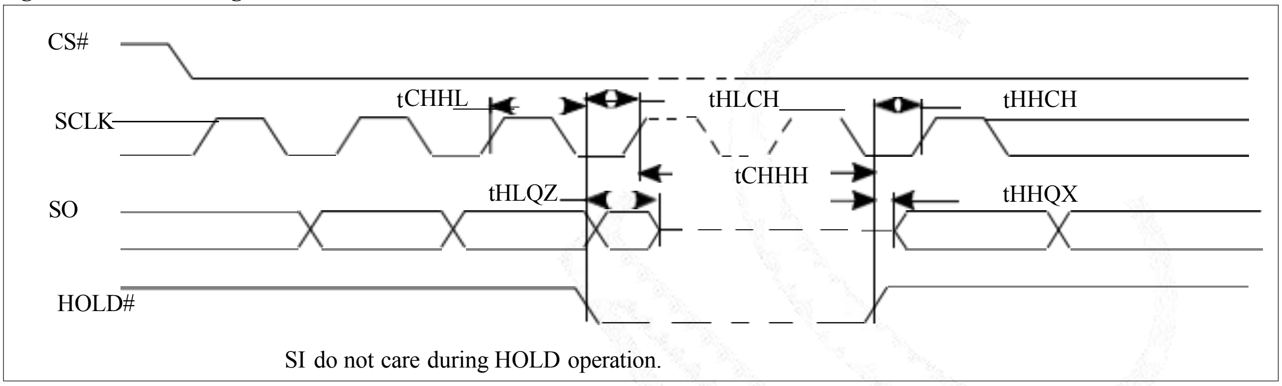
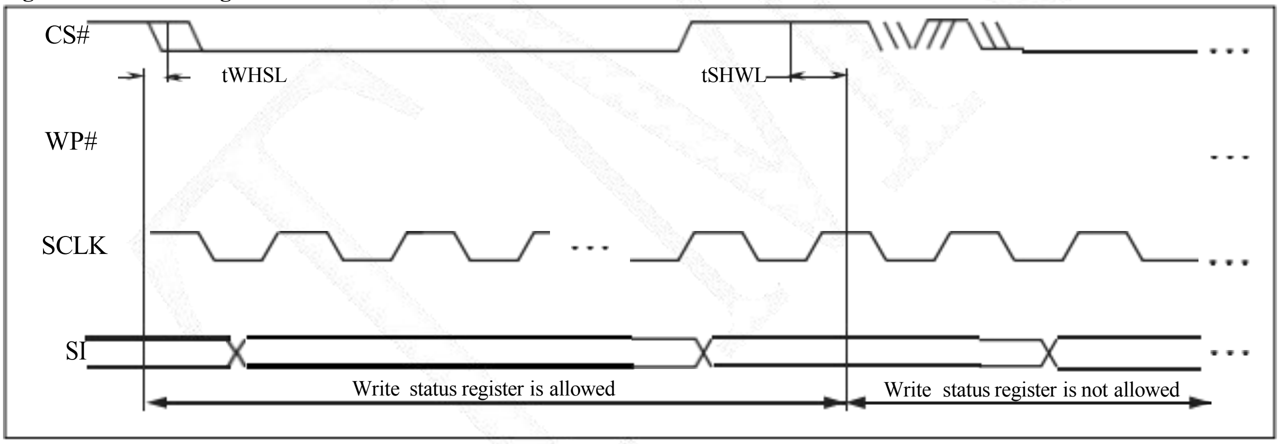


Figure 3-7 WP Timing



3.5. Operation Conditions

At Device Power-Up and Power-Down

AC timing illustrated in "Figure AC Timing at Device Power-Up" and "Figure Power-Down Sequence" are for the supply voltages and the control signals at device power-up and power-down. If the timing in the figures is ignored, the device will not operatecorrectly.

During power-up and power-down, CS# needs to follow the voltage applied on VCC to keep the device not to be selected. The CS# can be driven low when VCC reach Vcc(min.) and wait a period of tVSL.

Figure 3-8 AC Timing at Device Power-Up

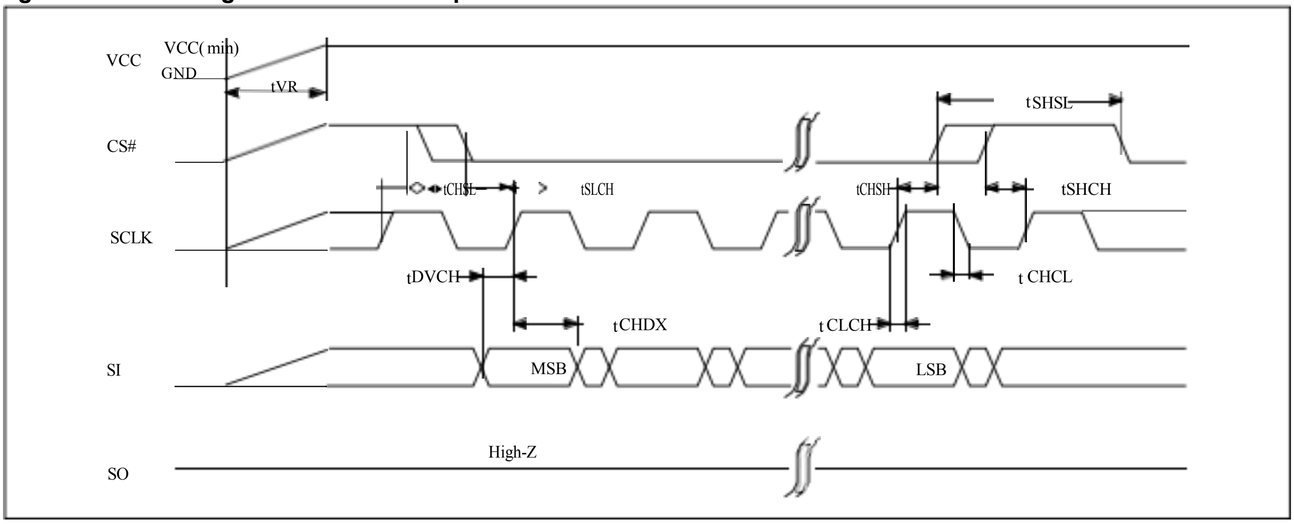
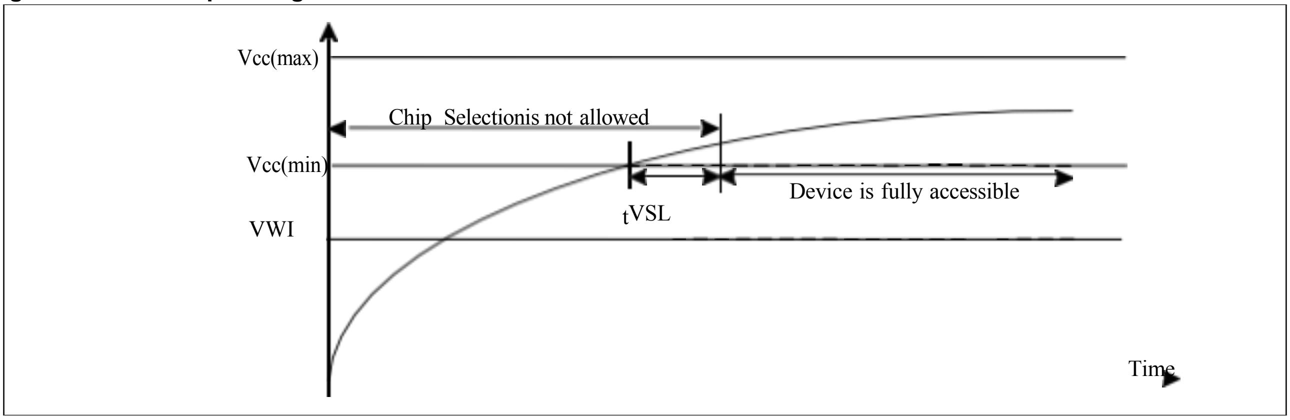


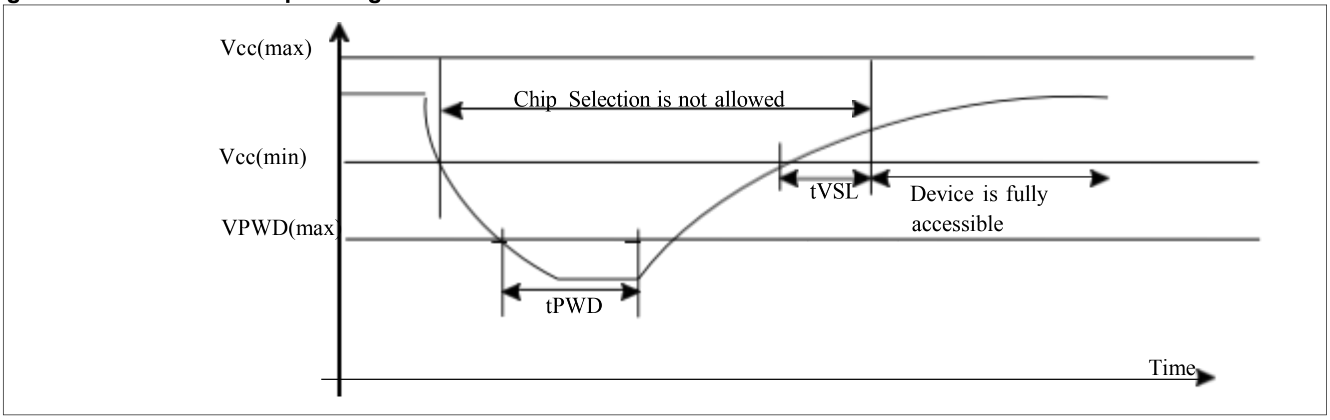
Figure 3-9 Power-Up Timing



Power Up/Down and Voltage Drop

For Power-down to Power-up operation, the VCC of flash device must below VPWD for at least tPWD timing. Please check the table below for more detail.

Figure 3-10 Power down-up Timing



Symbol	Parameter	min	max	unit
VPWD	VCC voltage needed to below VPWD for ensuring initialization will occur		1	V
tPWD	The minimum duration for ensuring initialization will occur	300		us
tVSL	VCC(min.) to device operation	70		us
tVR	VCC Rise Time	1	500000	us/V
VWI	Write Inhibit Voltage	1.45	1.55	V

4. Device Operation

4.1. Mode0 and Mode3

Before a command is issued, status register should be checked to ensure device is ready for the intended operation.

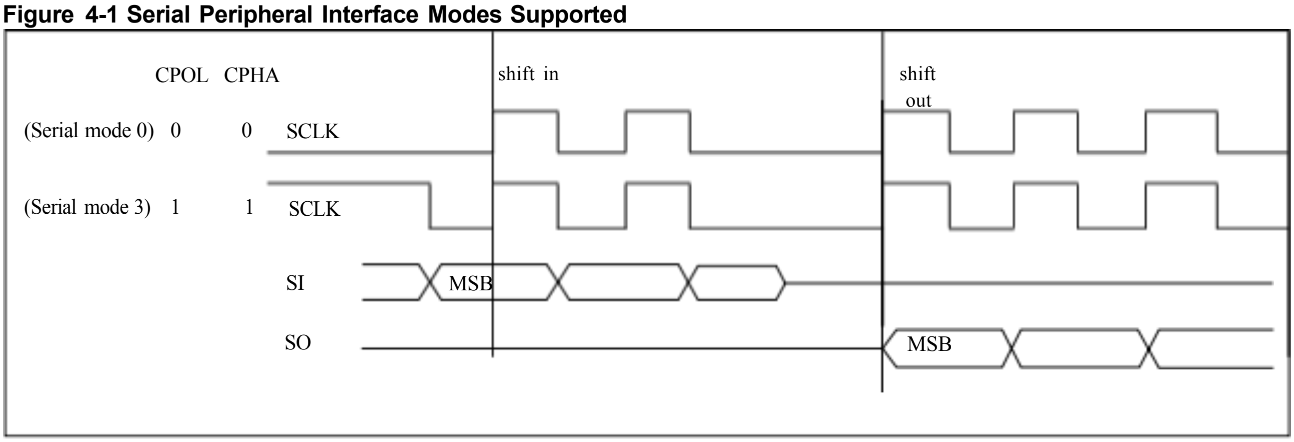
When incorrect command is inputted to this LSI, this LSI becomes standby mode and keeps the standby mode until next CS# falling edge. In standby mode, SO pin of this LSI should be High-Z. When correct command is inputted to this LSI, this LSI becomes active mode and keeps the active mode until next CS# rising edge.

Input data is latched on the rising edge of Serial Clock (SCLK) and data shifts out on the falling edge of SCLK.The difference of serial peripheral interface mode 0 and mode 3 is shown as Figure 9-1.

For the following instructions: RDID, RDSR, RDSR1, RDSCUR, READ, FAST_READ, DREAD, 2READ, 4READ, QREAD, RDSFDP, RES, REMS, DREMS, QREMS, the shifted-in instruction sequence is followed by a data-out sequence. After any bit of data being shifted out, the CS# can be high. For the following instructions: WREN, WRDI, WRSR, PE, SE, BE32K, BE, CE, PP, DPP, QPP, DP, ERSCUR, PRSCUR, SUSPEND, RESUME, RSTEN, RST, the CS# must go high exactly at the byte boundary; otherwise, the instruction will be rejected and not executed.

During the progress of Write Status Register, Program, Erase operation, to access the memory array is neglected and not affect the current operation of Write Status Register, Program, Erase.

Figure 4-1 Serial Peripheral Interface Modes Supported



Note:
CPOL indicates clock polarity of serial master, CPOL=1 for SCLK high while idle, CPOL=0 for SCLK low while not transmitting. CPHA indicates clock phase. The combination of CPOL bit and CPHA bit decides which serial mode is supported.

4.2. IO MODE

Standard SPI
The AL25WQ80 features a serial peripheral interface on 4 signals bus: Serial Clock (SCLK), Chip Select (CS#), Serial Data Input (SI) and Serial Data Output (SO). Both SPI bus mode 0 and 3 are supported. Input data is latched on the rising edge of SCLK and data shifts out on the falling edge of SCLK.

Dual SPI
The AL25WQ80 supports Dual SPI operation when using the “Dual Output Fast Read” and “Dual I/O Fast

Read"(3BHand BBH) commands. These commands allow data to be transferred to or from the device at two times the rate of the standard SPI. When using the Dual SPI command the SI and SO pins become bidirectional I/O pins: IO0 and IO1.

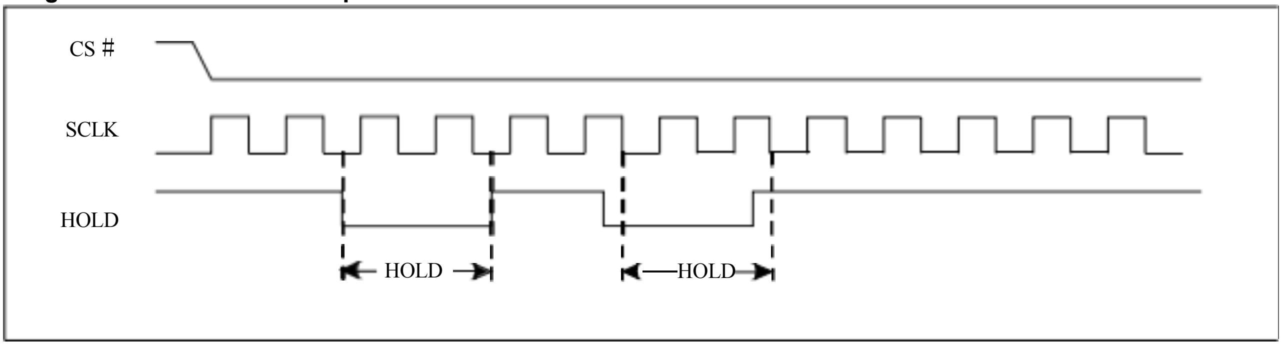
Quad SPI
The AL25WQ80 supports Quad SPI operation when using the "Quad Output Fast Read"," Quad I/O Fast Read"(6BH,EBH) commands. These commands allow data to be transferred to or from the device at four times the rate of the standard SPI. When using the Quad SPI command the SI and SO pins become bidirectional I/O pins: IO0 and IO1, and WP# and HOLD# pins become IO2 andIO3. Quad SPI commands require the non-volatile Quad Enable bit(QE) in Status Register to be set.

4.3. Hold Feature

HOLD# pin signal goes low to hold any serial communications with the device. The HOLD feature will not stop the operation of write status register, programming, or erasing in progress

The operation of HOLD requires Chip Select(CS#) keeping low and starts on falling edge of HOLD# pin signal while Serial Clock (SCLK) signal is being low (if Serial Clock signal is not being low, HOLD operation will not start until Serial Clock signal being low).The HOLD condition ends on the rising edge of HOLD# pin signal while Serial Clock(SCLK) signal is being low(if Serial Clock signal is not being low, HOLD operation will not end until Serial Clock being low).

Figure 4-2 Hold Condition Operation



During the HOLD operation, the Serial Data Output (SO) is high impedance when Hold# pin goes low and will keep high impedance until Hold# pin goes high. The Serial Data Input (SI) is don't care if both Serial Clock (SCLK) and Hold# pin goes low and will keep the state until SCLK goes low and Hold# pin goes high. If Chip Select (CS#) drives high during HOLD operation, it will reset the internal logic of the device. To re-start communication with chip, the HOLD# must be at high and CS# must be at low.

Note: The HOLD feature is disabled during Quad I/O mode.

4.4. Status Register

S15	S14	S13	S12	S11	S10	S9	S8
SUS1	CMP	LB3	LB2	LB1	SUS2	QE	SRP1

S7	S6	S5	S4	S3	S2	S1	S0
SRP0	BP4	BP3	BP2	BP1	BP0	WEL	WIP

The definition of the status register bits is as below:

WIP bit.

The Write in Progress (WIP) bit indicates whether the memory is busy in program/erase/write status register progress. When WIP bit sets to 1, means the device is busy in program/erase/write status register progress, when WIP bit sets 0, means the device is not in program/erase/write status register progress.

WEL bit.

The Write Enable Latch (WEL) bit indicates the status of the internal Write Enable Latch. When set to 1 the internal Write Enable Latch is set, when set to 0 the internal Write Enable Latch is reset and no Write Status Register, Program or Erase command isaccepted.

BP4, BP3, BP2, BP1, BP0 bits.

The Block Protect (BP4, BP3, BP2, BP1, and BP0) bits are non-volatile. They define the size of the area to be software protected against Program and Erase commands. These bits are written with the Write Status Register (WRSR) command. When the Block Protect (BP4, BP3, BP2, BP1, BP0) bits are set to 1, the relevant memory area (as defined in Table “Protected Area Sizes”).becomes protected against Page Program (PP), Page Erase (PE), Sector Erase (SE) and Block Erase (BE) commands. The Block Protect (BP4, BP3, BP2, BP1, and BP0) bits can be written provided that the Hardware Protected mode has not been set. The Chip Erase (CE) command is executed, only if the Block Protect (BP4, BP3, BP2, BP1and BP0) are set to “None protected”.

SRP1, SRP0 bits.

The Status Register Protect (SRP1 and SRP0) bits are non-volatile Read/Write bits in the status register. The SRP bits control the method of write protection: software protection, hardware protection, power supply lock-down or one time programmable protection

SRP1	SRP0	WP#	Status Register	Description
0	0	x	Software Protected	The Status Register can be written to after a Write Enable command, WEL=1.(Default)
0	1	0	Hardware Protected	WP#=0, the Status Register locked and can not be write to.
0	1	1	Hardware Unprotected	WP#=1, the Status Register is unlocked and can be written to after a Write Enable command, WEL=1.
1	0	x	Power Supply Lock-Down(1)	Status Register is protected and can not be written to again until the next Power-Down, Power-Up cycle.
1	1	x	One Time Program(2)	Status Register is permanently protected and can not be written to.

NOTE:

1. When SRP1, SRP0=(1, 0), a Power-Down, Power-Up cycle will change SRP1, SRP0 to (0, 0) state.
2. This feature is available on special order. Please contact Along fordetails.

QE bit.

The Quad Enable (QE) bit is a non-volatile Read/Write bit in the Status Register that allows Quad operation. When the QE bit is set to 0 (Default) the WP# pin and HOLD# pin are enable. When the QE pin is set to 1, the Quad IO2 and IO3 pins are enabled. (The QE bit should never be set to 1 during standard SPI or Dual SPI operation if the WP# or HOLD# pins are tied directly to the power supply or ground)

LB3, LB2, LB1, bits.

The LB3, LB2, LB1, bits are non-volatile One Time Program (OTP) bits in Status Register (S13-S11) that provide the write protect control and status to the Security Registers. The default state of LB3-LB1are0, the security registers are unlocked. The LB3-LB1bitscan be set to 1 individually using the Write Register instruction. The LB3-LB1bits are One Time Programmable, once its set to 1, the Security Registers will become read-only permanently.

CMP bit

The CMP bit is a non-volatile Read/Write bit in the Status Register(S14). It is used in conjunction the BP4-BP0 bits to provide more flexibility for the array protection. Please see the table "Protected Area Size" for details. The default setting is CMP=0.

SUS1, SUS2bit

The SUS1 and SUS2bit are read only bit in the status register (S15and S10) that are set to 1 after interrupting an program/erase/write status register progress by Program/Erase Suspend (75H or B0H) command (The Erase Suspend will set the SUS1 to 1,and the Program Suspend will set the SUS2 to 1). The SUS1 and SUS2 bit are cleared to 0 by Program/Erase Resume (7AH or 30H) command as well as a power-down, power-up cycle.

4.5. Configure Register

S7	S6	S5	S4	S3	S2	S1	S0
DP	Reserved	Reserved	Reserved	Reserved	Reserved	Reserve	Reserved

The definition of the configure register bits is as below:

DP bit.

The Dual Page (DP) bit is a non-volatile Read/Write bit in the Configure Register that allows Dual Page operation. When the DP bit is set to 0 (Default) the page size is 256bytes. When the DP pin is set to 1, the page size is 512bytes.

This bit controls the page programming buffer address wrap point. Legacy SPI devices generally have used a 256 Byte page programming buffer and defined that if data is loaded into the buffer beyond the 255 Byte location, the address at which additional bytes are loaded would be wrapped to address zero of the buffer. The P25Q08U provides a 512 Byte page programming buffer that can increase programming performance. For legacy software compatibility, this configuration bit provides the option to continue the wrapping behavior at the 256 Byte boundary or to enable full use of the available 512 Byte buffer by not wrapping the load address at the 256 Byte boundary.

When the DP pin is set to 1, the page erase instruction (81h) will erase the data of the chosen Dual Page to be "1".

4.6. Data Protection

During power transition, there may be some false system level signals which result in inadvertent erasure or programming. The device is designed to protect itself from these accidental write cycles.

The state machine will be reset as standby mode automatically during power up. In addition, the control register architecture of the device constrains that the memory contents can only be changed after specific command sequences have completed successfully.

In the following, there are several features to protect the system from the accidental write cycles during VCC power-up and power-down or from system noise.

- Power-on reset: to avoid sudden power switch by system power supply transition, the power-on reset may protect the Flash.
- Valid command length checking: The command length will be checked whether it is at byte base and completed on byte boundary.
- Write Enable (WREN) command: WREN command is required to set the Write Enable Latch bit (WEL) before issuing other commands to change data.
- Software Protection Mode: The Block Protect (BP4, BP3, BP2, BP1, and BP0) bits define the section of the memory array that can be read but not change.
- Hardware Protection Mode: WP# going low to protected the BP0~BP4bits and SRP0~1bits
- Deep Power-Down Mode: By entering deep power down mode, the flash device is under protected from writing all commands except the Release form Deep Power-Down Mode command.

Table 4-1. Protected Area Sizes

AL25WQ80 Protected Area Sizes (CMP bit = 0)

Status bit					Memory Content			
BP4	**BP3**	**BP2**	**BP1**	**BP0**	**Blocks**	**Addresses**	**Density**	**Portion**
x	x	0	0	0	NONE	NONE	NONE	NONE
0	0	0	0	1	15	0F0000H-0FFFFFH	64KB	Upper 1/16
0	0	0	1	0	14 and 15	0E0000H-0FFFFFH	128KB	Upper 1/8
0	0	0	1	1	12 to 15	0C0000H-0FFFFFH	256KB	Upper 1/4
0	0	1	0	0	8 to 15	080000H-0FFFFFH	512KB	Upper 1/2
0	1	0	0	1	0	000000H-00FFFFH	64KB	Lower 1/16
0	1	0	1	0	0 and 1	000000H-01FFFFH	128KB	Lower 1/8
0	1	0	1	1	0 to 3	000000H-03FFFFH	256KB	Lower 1/4
0	1	1	0	0	0 to 7	000000H-07FFFFH	512KB	Lower 1/2
0	x	1	0	1	0 to 15	000000H-0FFFFFH	1MB	ALL
x	x	1	1	x	0 to 15	000000H-0FFFFFH	1MB	ALL
1	0	0	0	1	15	0FF000H-0FFFFFH	4KB	Upper 1/256
1	0	0	1	0	15	0FE000H-0FFFFFH	8KB	Upper 1/128
1	0	0	1	1	15	0FC000H-0FFFFFH	16KB	Upper 1/64
1	0	1	0	x	15	0F8000H- 0FFFFFH	32KB	Upper 1/32
1	1	0	0	1	0	000000H-000FFFH	4KB	Lower 1/256
1	1	0	1	0	0	000000H-001FFFH	8KB	Lower 1/128
1	1	0	1	1	0	000000H-003FFFH	16KB	Lower 1/64
1	1	1	0	x	0	000000H-007FFFH	32KB	Lower 1/32

AL25WQ80 Protected Area Sizes (CMP bit = 1)

Status bit					Memory Content			
BP4	**BP3**	**BP2**	**BP1**	**BP0**	**Blocks**	**Addresses**	**Density**	**Portion**
x	x	0	0	0	0 to 15	000000H-0FFFFFH	1MB	ALL
0	0	0	0	1	0 to 14	000000H-0EFFFFH	960KB	Lower 15/16
0	0	0	1	0	0 to 13	000000H-0DFFFFH	896KB	Lower 7/8
0	0	0	1	1	0 to 11	000000H-0BFFFFH	768KB	Lower 3/4
0	0	1	0	0	0 to 7	000000H-07FFFFH	512KB	Lower 1/2
0	1	0	0	1	1 to 15	010000H-0FFFFFH	960KB	Upper 15/16
0	1	0	1	0	2 to 15	020000H-0FFFFFH	896KB	Upper 7/8
0	1	0	1	1	4 to 15	040000H-0FFFFFH	768KB	Upper 3/4
0	1	1	0	0	8 to 15	080000H-0FFFFFH	512KB	Upper 1/2
0	x	1	0	1	NONE	NONE	NONE	NONE
x	x	1	1	x	NONE	NONE	NONE	NONE
1	0	0	0	1	0 to 15	000000H-0FEFFFH	1020KB	Lower 255/256
1	0	0	1	0	0 to 15	000000H-0FDFFFH	1016KB	Lower 127/128
1	0	0	1	1	0 to 15	000000H-0FBFFFH	1008KB	Lower 63/64
1	0	1	0	x	0 to 15	000000H-0F7FFFH	992KB	Lower 31/32
1	1	0	0	1	0 to 15	001000-0FFFFFH	1020KB	Upper 255/256
1	1	0	1	0	0 to 15	002000-0FFFFFH	1016KB	Upper 127/128
1	1	0	1	1	0 to 15	004000-0FFFFFH	1008KB	Upper 63/64
1	1	1	0	x	0 to 15	008000-0FFFFFH	992KB	Upper 31/32

Note:

1. X=don’t care
2. If any erase or program command specifies a memory that contains protected data portion, this command will be ignored.

5. Commands

5.1. Commands listing

Commands	Abbr.	Code	ADR Bytes	DMY Bytes	Data Bytes	Function description
Read						
Read Array (fast)	FREAD	0Bh	3	1	1+	n bytes read out until CS# goes high
Read Array (low power)	READ	03h	3	0	1+	n bytes read out until CS# goes high
Read Dual Output	DREAD	3Bh	3	1	1+	n bytes read out by Dual output
Read 2x I/O	2READ	BBh	3	1	1+	n bytes read out by 2 x I/O
Read Quad Output	QREAD	6Bh	3	1	1+	n bytes read out by Quad output
Read 4x I/O	4READ	EBh	3	1	1+	n bytes read out by 4 x I/O
Program and Erase						
Page Erase	PE	81h	3	0	0	erase selected page
Sector Erase (4K bytes)	SE	20h	3	0	0	erase selected sector
Block Erase (32K bytes)	BE32	52h	3	0	0	erase selected 32K block
Block Erase (64K bytes)	BE64	D8h	3	0	0	erase selected 64K block
Chip Erase	CE	60h	0	0	0	erase whole chip
		C7h	0	0	0	erase whole chip
Page Program	PP	02h	3	0	1+	program selected page
Dual-IN Page Program	2PP	A2h	3	0	1+	program selected page by Dual input
Quad page program	QPP	32h	3	0	1+	quad input to program selected page
Program/Erase Suspend	PES	75h	0	0	0	suspend program/erase operation
		B0h	0	0	0	suspend program/erase operation
Program/Erase Resume	PER	7Ah	0	0	0	continue program/erase operation
		30h	0	0	0	continue program/erase operation
Protection						
Write Enable	WREN	06h	0	0	0	sets the (WEL) write enable latch bit
Write Disable	WRDI	04h	0	0	0	resets the (WEL) write enable latch bit
Volatile SR Write Enable	VWREN	50h	0	0	0	Write enable for volatile status register
Security						
Erase Security Registers	ERSCUR	44h	3	0	0	Erase security registers
Program Security Registers	PRSCUR	42h	3	0	1+	Program security registers
Read Security Registers	RDSCUR	48h	3	1	1+	Read value of security register
Status Register						
Read Status Register	RDSR	05h	0	0	1	read out status register
	RDSR2	35h	0	0	1	Read out status register-1
Read Configure Register	RDCR	15h	0	0	1	read out configureregister
Active Status Interrupt	ASI	25h	0	1	0	Enable the active status interrupt

Figure 5-1 Command set

Command set (Cont'd)

Commands	Abbr.	Code	ADR Bytes	DMY Bytes	Data Bytes	Function
Other Commands						
Write Status Register	WRSR	01h	0	0	2	Write data to status registers
Write Configure Register	WRCR	31h	0	0	1	Write data to configuration registers
Reset Enable	RSTEN	66h	0	0	0	Enable reset
Reset	RST	99h	0	0	0	Reset
Read Manufacturer/device ID	RDID	9Fh	0	0	1 to 3	output JEDEC ID: 1-byte manufacturer ID & 2-byte device ID
Read Manufacture ID	REMS	90h	3		1+	Read manufacturer ID/device ID data
Dual Read Manufacture ID	DREMS	92h	3	1	1+	Dual output read manufacture/device ID
Quad Read Manufacture ID	QREMS	94h	3	1	1+	Quad output read manufacture/device ID
Deep Power-down	DP	B9h	0	0	0	enters deep power-down mode
Release Deep Power-down/Read Electronic ID	RDP/RES	ABh	3	0	1	Read electronic ID data
Set burst length	SBL	77h	0	0	0	Set burst length
Read SFDP	RDSFDP	5Ah				Read SFDP parameter
Release read enhanced		FFh				Release from read enhanced
Read unique ID	RUID	4Bh		4	1+	Read unique ID

NOTE:

1. Dual Output data
IO0 = (D6, D4, D2, D0)
IO1 = (D7, D5, D3, D1)

2. Dual Input Address
IO0 = A22, A20, A18, A16, A14, A12, A10, A8 A6, A4, A2, A0, M6, M4, M2, M0 IO1
= A23, A21, A19, A17, A15, A13, A11, A9 A7, A5, A3, A1, M7, M5, M3, M1

3. Quad Output Data
IO0 = (D4, D0, ...)
IO1 = (D5, D1, ...)
IO2 = (D6, D2, ...)
IO3 = (D7, D3,.....)

4. Quad Input Address
IO0 = A20, A16, A12, A8, A4, A0, M4, M0
IO1 = A21, A17, A13, A9, A5, A1, M5, M1
IO2 = A22, A18, A14, A10, A6, A2, M6, M2
IO3 = A23, A19, A15, A11, A7, A3, M7, M3

5. Fast Read Quad I/O Data

IO0 = (x, x, x, x, D4, D0,…)
IO1 = (x, x, x, x, D5, D1,…)
IO2 = (x, x, x, x, D6, D2,…)
IO3 = (x, x, x, x, D7, D3,…)

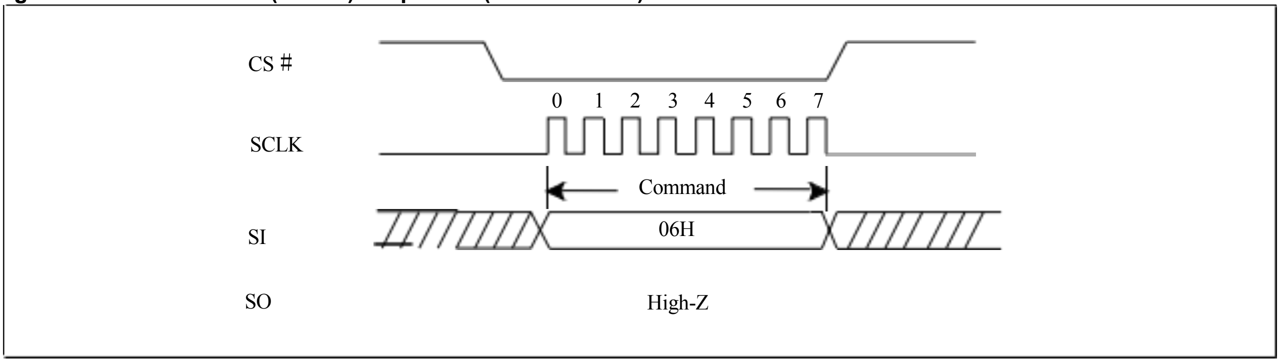
6. Security Registers Address:
Security Register1: A23-A16=00H, A15-A9=0001000, A8-A0= Byte Address;
Security Register2: A23-A16=00H, A15-A9=0010000, A8-A0= Byte Address;
Security Register3: A23-A16=00H, A15-A9=0011000, A8-A0= Byte Address;

5.2. Write Enable (WREN)

The Write Enable (WREN) instruction is for setting Write Enable Latch (WEL) bit. For those instructions like PP,DPP,QPP, PE,SE, BE32K,BE, CE, and WRSR,ERSCUR, PRSCUR which are intended to change the device content, should be set every time after the WREN instruction setting the WEL bit.

The sequence of issuing WREN instruction is: CS# goes low→ sending WREN instruction code→ CS# goes high.

Figure 5-2 Write Enable (WREN) Sequence (Command 06)



5.3.Write Disable (WRDI)

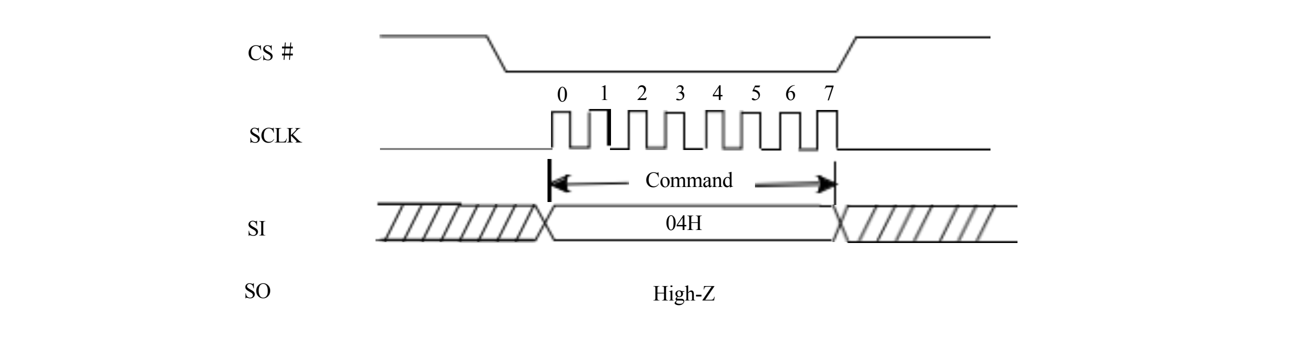
The Write Disable (WRDI) instruction is for resetting Write Enable Latch (WEL) bit.

The sequence of issuing WRDI instruction is: CS# goes low→ sending WRDI instruction code→ CS# goes high.

The WEL bit is reset by following situations:

- Power-up
- Write Disable (WRDI) instructioncompletion
- Write Status Register (WRSR) instruction completion
- Page Program (PP) instruction completion
- Dual Input Page Program (DPP) instructioncompletion
- Quod Page Program (QPP) instructioncompletion
- Page Erase (PE) instruction completion
- Sector Erase (SE) instructioncompletion
- Block Erase (BE32K,BE) instructioncompletion
- Chip Erase (CE) instruction completion
- Erase Security Register (ERSCUR) instruction completion
- Program Security Register (PRSCUR) instruction completion
- Reset (RST) instructioncompletion

Figure 5-3 Write Disable (WRDI) Sequence (Command 04)

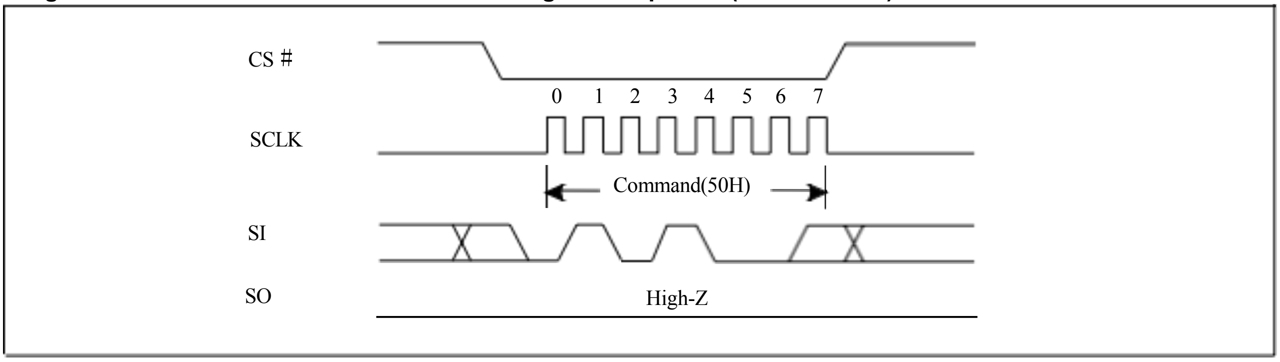


5.4. Write Enable for Volatile Status Register

The non-volatile Status Register bits can also be written to as volatile bits. This gives more flexibility to change the system configuration and memory protection schemes quickly without waiting for the typical non-volatile bit write cycles or affecting the endurance of the Status Register non-volatile bits. The Write Enable for Volatile Status Register command must be issued prior to a Write Status Register command. The Write Enable for Volatile Status Register command will not set the Write Enable Latch bit, it is only valid for the Write Status Register command to change the volatile Status Register bit values.

The sequence of issuing Write Enable for Volatile Status Register instruction is: CS# goes low→ sending Write Enable for Volatile Status Register instruction code→ CS# goes high.

Figure 5-4 Write Enable for Volatile Status Register Sequence (Command 50)



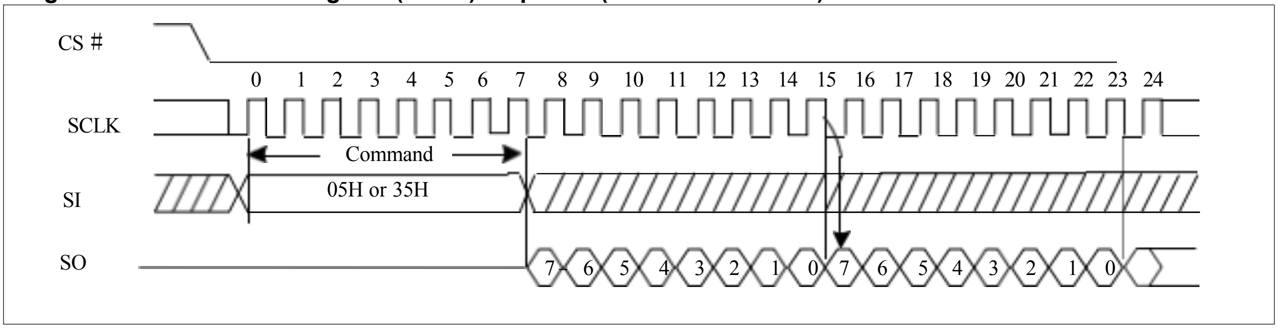
5.5. Read Status Register (RDSR)

The RDSR instruction is for reading Status Register Bits. The Read Status Register can be read at any time (even in program/erase/write status register condition). It is recommended to check the Write in Progress (WIP) bit before sending a new instruction when a program, erase, or write status register operation is in progress. For command code “05H”, the SO will output Status Register bits S7~S0. The command code “35H” , theSO will output Status Register bits S15~S8.

The sequence of issuing RDSR instruction is: CS# goes low→ sending RDSR instruction code→ Status Register data out on SO.

The SIO[3:1] are "don't care".

Figure 5-5 Read Status Register (RDSR) Sequence (Command 05 or 35)



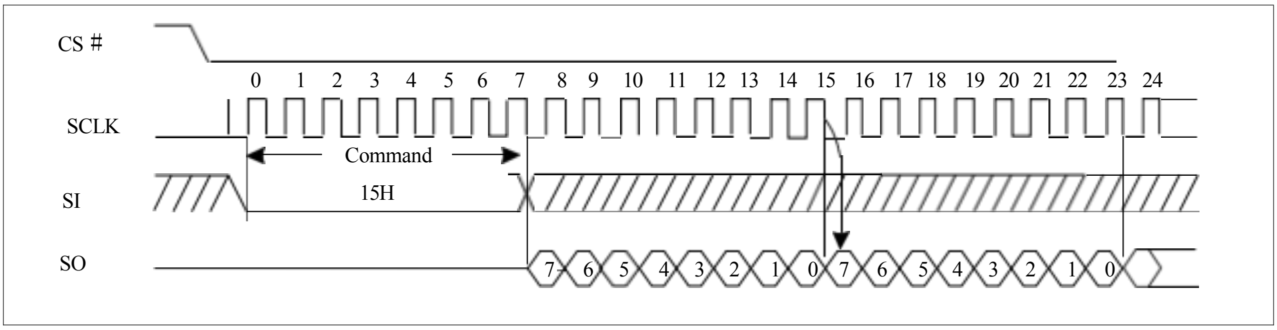
5.6.Read Configure Register (RDCR)

The RDCR instruction is for reading Configure Register Bits. The Read Configure Register can be read at any time (even in program/erase/write status register condition). It is recommended to check the Write in Progress (WIP) bit before sending a new instruction when a program, erase, or write status register operation is in progress.

The sequence of issuing RDCR instruction is: CS# goes low→ sending RDCR instruction code→ Configure Register data out on SO.

The SIO[3:1] are "don't care".

Figure 5-6 Read Configure Register (RDCR) Sequence (Command 15)



5.7. Active Status Interrupt (ASI)

To simplify the readout of the WIP bit, the Active Status Interrupt command (25h) may be used. It is then not necessary to continuously read the status register, it is sufficient to monitor the value of the SO line. If the SO line is connected to an interrupt line on the host controller, the host controller may be in sleep mode until the SO line indicates that the device is ready for the next command.

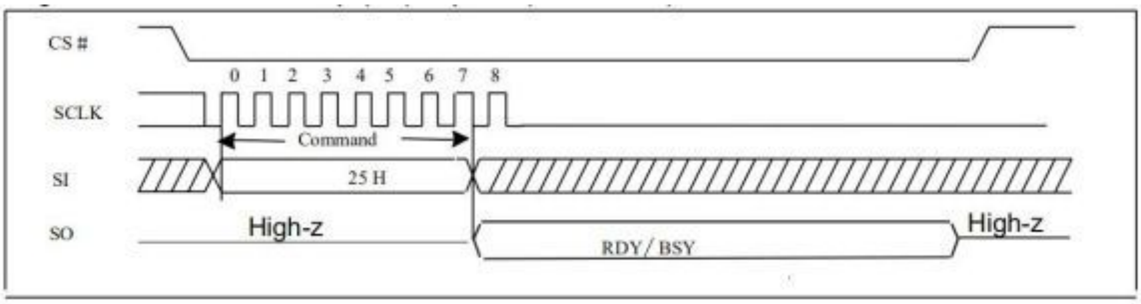
The WIP bit can be read at any time, including during an internally self-timed program or erase operation. To enable the Active Status Interrupt command, the CS pin must first be asserted and the opcode of 25h must be clocked into the device. For SPI Mode0 and Mode3, at least one dummy bit has to be clocked into the device after the last bit of the opcode has been clocked in. (In most cases, this is most easily done by sending a dummy byte to the device.) The value of the SI line after the opcode is clocked in is of no significance to the operation.

The value of WIP is then output on the SO line, and is continuously updated by the device for as long as the CS pin remains asserted. Additional clocks on the SCLK pin are not required. For SPI Mode3, SCLK must keep low. If the WIP bit changes from 1 to 0 while the CS pin is asserted, the SO line will change from 1 to 0. (The WIP bit cannot change from 0 to 1 during an operation, so if the SO line already is 0, it will not change.)

Deasserting the CS pin will terminate the Active Status Interrupt operation and put the SO pin into a high-impedance state. The CS pin can be deasserted at any time and does not require that a full byte of data be read.

The sequence of issuing ASI instruction is: CS# goes low→ sending ASI instruction code→ WIP data out on SO.

Figure 5-7 Active Status Interrupt (ASI) Sequence (Command 25)



5.8. Write Status Register (WRSR)

The Write Status Register (WRSR) command allows new values to be written to the Status Register. Before it can be accepted, a Write Enable (WREN) command must previously have been executed. After the Write Enable (WREN) command has been decoded and executed, the device sets the Write Enable Latch (WEL).

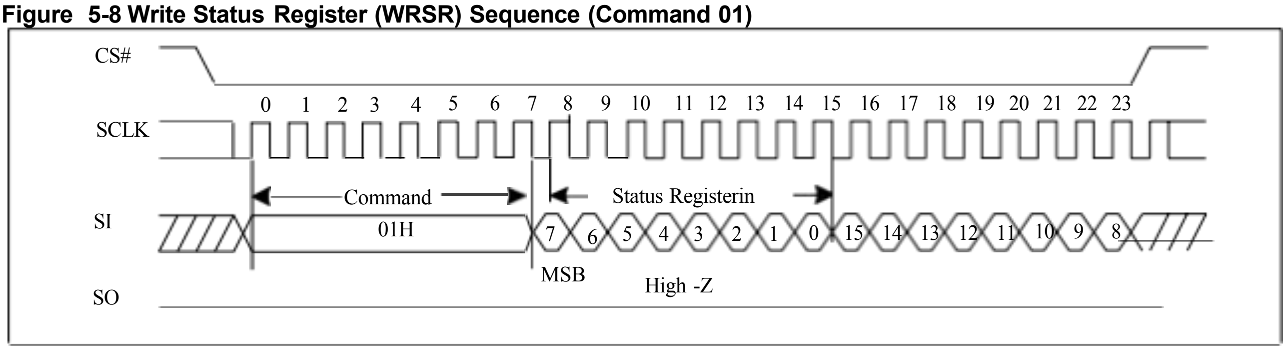
The Write Status Register (WRSR) command has no effect on S15, S10, S1 and S0 of the Status Register. CS# must be driven high after the eighth or sixteen bit of the data byte has been latched in. If not, the Write Status Register (WRSR) command is not executed. If CS# is driven high after eighth bit of the data byte, the CMP and QE and SRP1 bits will not change. As soon as CS# is driven high, the self-timed Write Status Register cycle (whose duration is tW) is initiated. While the Write Status Register cycle is in progress, the Status Register may still be read to check the value of the Write In Progress (WIP) bit. The Write In Progress (WIP) bit is 1 during the self-timed Write Status Register cycle, and is 0 when it is completed. When the cycle is completed, the Write Enable Latch (WEL) is reset.

The Write Status Register (WRSR) command allows the user to change the values of the Block Protect (BP4, BP3, BP2, BP1, and BP0) bits, to define the size of the area that is to be treated as read-only, as defined in Table1. The Write Status Register (WRSR) command also allows the user to set or reset the Status Register Protect (SRP1 and SRP0) bits in accordance with the Write Protect (WP#) signal. The Status Register Protect (SRP1 and SRP0) bits and Write Protect (WP#) signal allow the device to be put in the Hardware Protected Mode. The Write Status Register (WRSR) command is not executed once the Hardware Protected Mode is entered.

The sequence of issuing WRSR instruction is: CS# goes low→ sending WRSR instruction code→ Status Register data on SI→CS# goes high.

The CS# must go high exactly at the 8 bits or 16 bits data boundary; otherwise, the instruction will be rejected and not executed. The self-timed Write Status Register cycle time (tW) is initiated as soon as Chip Select (CS#) goes high. The Write in Progress (WIP) bit still can be checked during the Write Status Register cycle is in progress. The WIP sets 1 during the tW timing, and sets 0 when Write Status Register Cycle is completed, and the Write Enable Latch (WEL) bit is reset.

Figure 5-8 Write Status Register (WRSR) Sequence (Command 01)



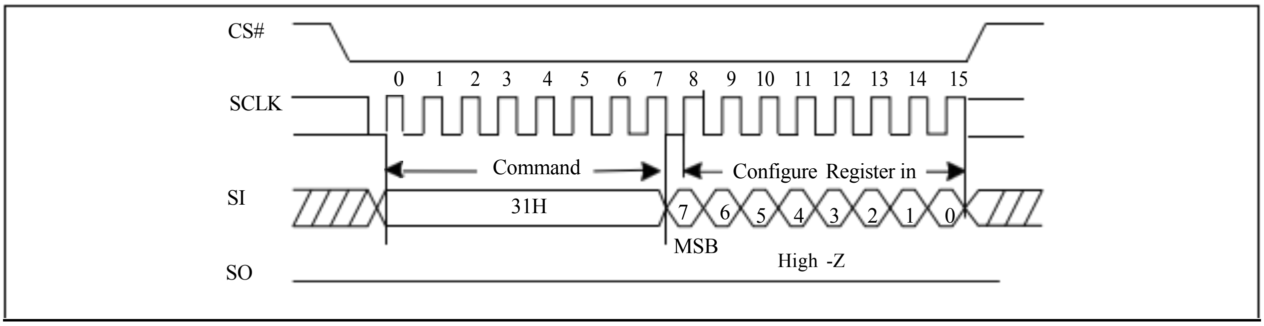
5.9. Write Configure Register (WRCR)

The Write Configure Register (WRCR) command allows new values to be written to the Configure Register. Before it can be accepted, a Write Enable (WREN) command must previously have been executed. After the Write Enable (WREN) command has been decoded and executed, the device sets the Write Enable Latch (WEL).

The sequence of issuing WRCR instruction is: CS# goes low→ sending WRCR instruction code→ Configure Register data on SI→CS# goes high.

The CS# must go high exactly at the 8 bits data boundary; otherwise, the instruction will be rejected and not executed. The self-timed Write Status Register cycle time (tW) is initiated as soon as Chip Select (CS#) goes high. The Write in Progress (WIP) bit still can be checked during the Write Status Register cycle is in progress. The WIP sets 1 during the tW timing, and sets 0 when Write Configure Register Cycle is completed, and the Write Enable Latch (WEL) bit is reset.

Figure 5-9 Write Configure Register (WRCR) Sequence (Command 01)

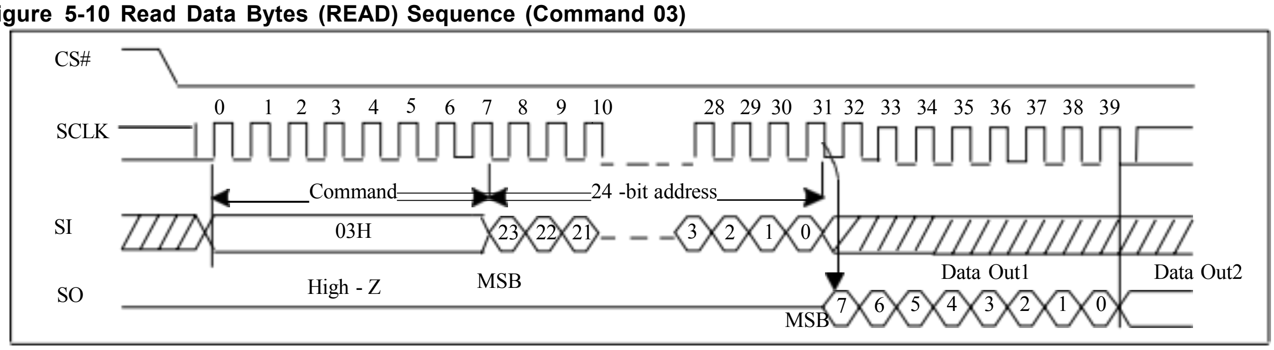


5.10. Read Data Bytes (READ)

The read instruction is for reading data out. The address is latched on rising edge of SCLK, and data shifts out on the falling edge of SCLK at a maximum frequency fR. The first address byte can be at any location. The address is automatically increased to the next higher address after each byte data is shifted out, so the whole memory can be read out at a single READ instruction. The address counter rolls over to 0 when the highest address has been reached.

The sequence of issuing READ instruction is: CS# goes low→ sending READ instruction code→ 3-byte address on SI→ data out on SO→ to end READ operation can use CS# to high at any time during data out.

Figure 5-10 Read Data Bytes (READ) Sequence (Command 03)



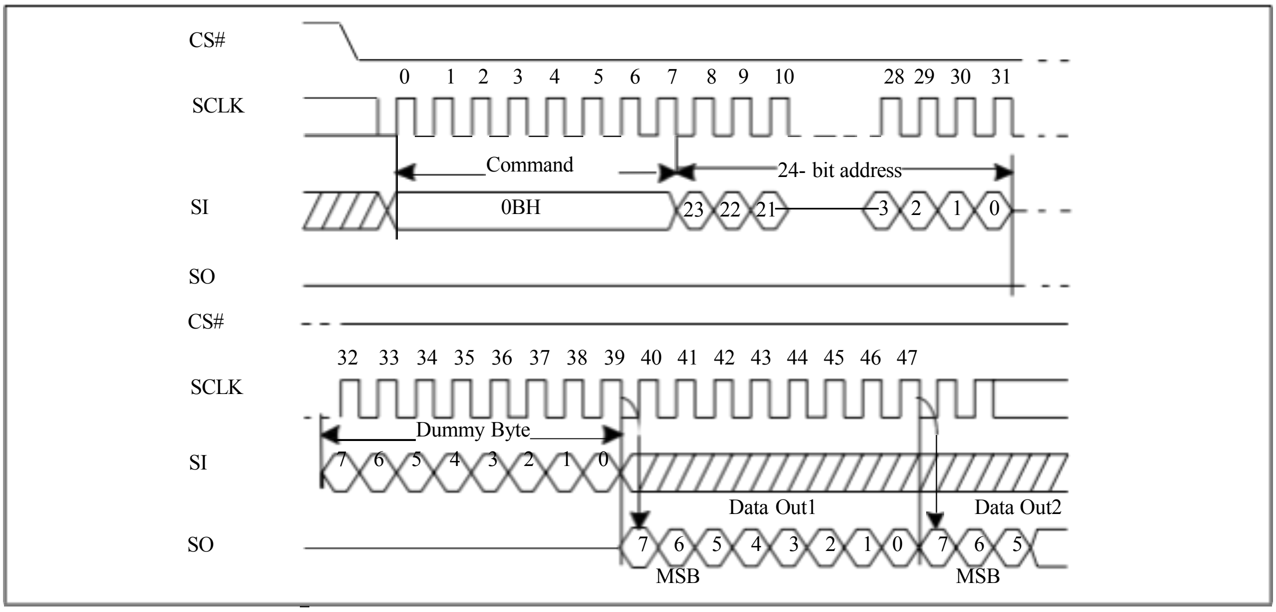
5.11. Read Data Bytes at Higher Speed(FAST_READ)

The FAST_READ instruction is for quickly reading data out. The address is latched on rising edge of SCLK, and data of each bit shifts out on the falling edge of SCLK at a maximum frequency fC. The first address byte can be at any location. The address is automatically increased to the next higher address after each byte data is shifted out, so the whole memory can be read out at a single FAST_READ instruction. The address counter rolls over to 0 when the highest address has been reached.

The sequence of issuing FAST_READ instruction is: CS# goes low→ sending FAST_READ instruction code→3-byte address on SI→ 1-dummy byte address on SI→data out on SO→ to end FAST_READ operation can use CS# to high at any time during data out.

While Program/Erase/Write Status Register cycle is in progress, FAST_READ instruction is rejected without any impact on the Program/Erase/Write Status Register current cycle.

Figure 5-11 Read at Higher Speed (FAST_READ) Sequence (Command 0B)


CS#
SCLK
SI
SO
0 1 2 3 4 5 6 7 8 9 10 28 29 30 31
Command
24- bit address
0BH
23 22 21 3 2 1 0
CS#
SCLK
SI
SO
32 33 34 35 36 37 38 39 40 41 42 43 44 45 46 47
Dummy Byte
7 6 5 4 3 2 1 0
Data Out1
Data Out2
7 6 5 4 3 2 1 0 7 6 5
MSB
MSB

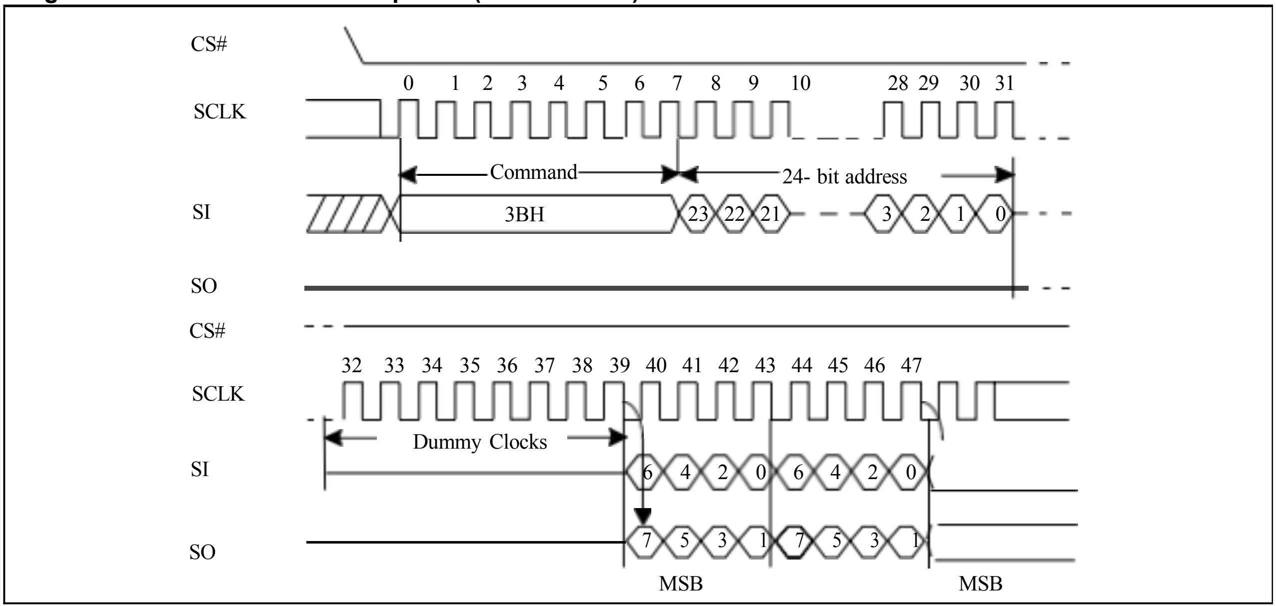
5.12. Dual Read Mode (DREAD)

The DREAD instruction enable double throughput of Serial NOR Flash in read mode. The address is latched on rising edge of SCLK, and data of every two bits (interleave on 2 I/O pins) shift out on the falling edge of SCLK at a maximum frequency fT. The first address byte can be at any location. The address is automatically increased to the next higher address after each byte data is shifted out, so the whole memory can be read out at a single DREAD instruction. The address counter rolls over to 0 when the highest address has been reached. Once writing DREAD instruction, the following data out will perform as 2-bit instead of previous 1-bit.

The sequence of issuing DREAD instruction is: CS# goes low → sending DREAD instruction → 3-byte address on SI → 8-bit dummy cycle → data out interleave on SIO1 & SIO0 → to end DREAD operation can use CS# to high at any time during data out.

While Program/Erase/Write Status Register cycle is in progress, DREAD instruction is rejected without any impact on the Program/Erase/Write Status Register current cycle.

Figure 5-12 Dual Read Mode Sequence (Command 3B)



5.13. 2 X IO Read Mode(2READ)

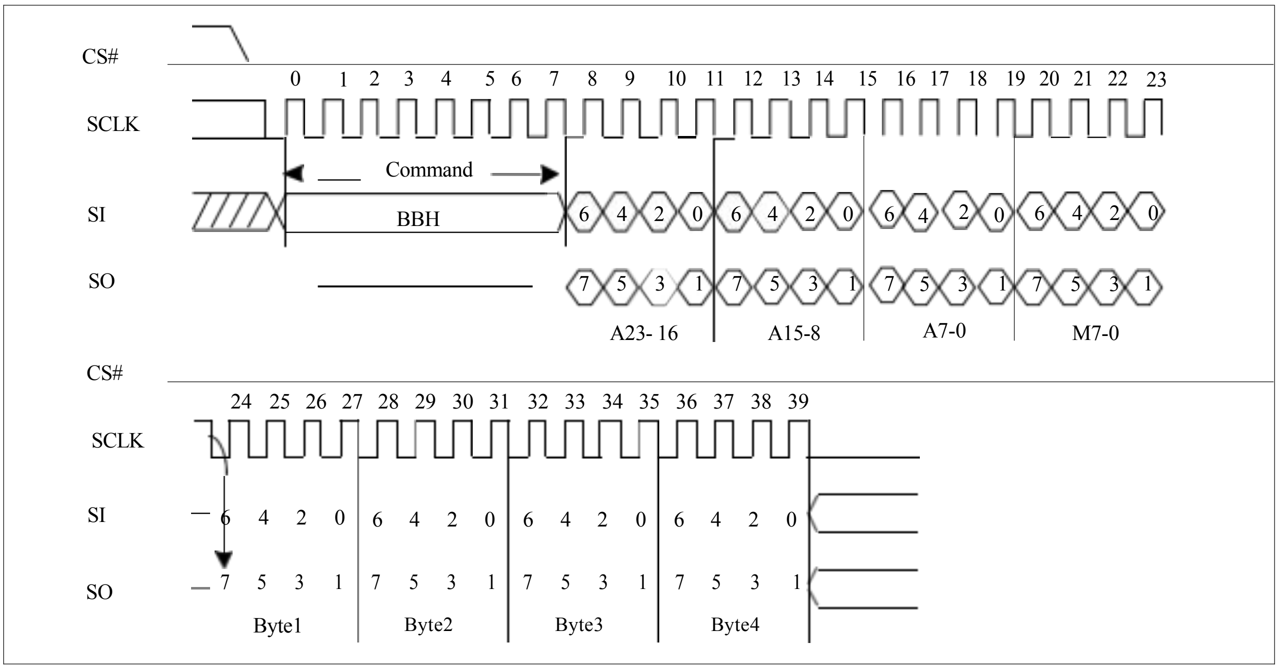
The 2READ instruction enables Double Transfer Rate of Serial NOR Flash in read mode. The address is latched on rising edge of SCLK, and data of every two bits (interleave on 2 I/O pins) shift out on the falling edge of SCLK at a maximum frequency fT. The first address byte can be at any location. The address is automatically increased to the next higher address after each byte data is shifted out, so the whole memory can be read out at a single 2READ instruction. The address counter rolls over to 0 when the highest address has been reached.

Once writing 2READ instruction, the following address/dummy/data out will perform as 2-bit instead of previous 1-bit.

The sequence of issuing 2READ instruction is: CS# goes low→ sending 2READ instruction→ 24-bit address interleave on SIO1 & SIO0→ 8-bit dummy cycle on SIO1 & SIO0→ data out interleave on SIO1 & SIO0→ to end 2READ operation can use CS# to high at any time during data out.

While Program/Erase/Write Status Register cycle is in progress, 2READ instruction is rejected without any impact on the Program/Erase/Write Status Register current cycle.

Figure 5-13 2 X IO Read Mode Sequence (Command BB M5-4 ≠ (1,0))

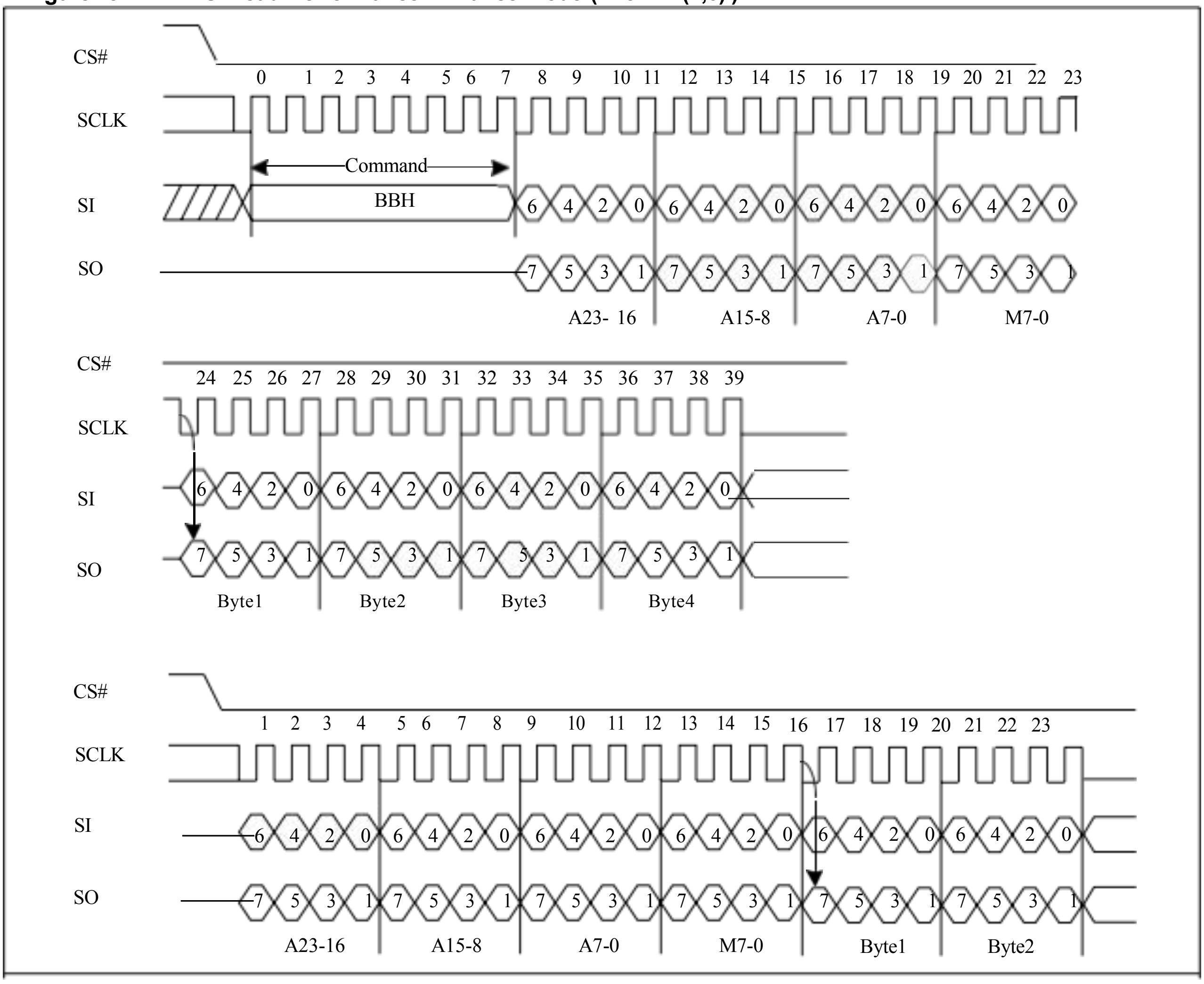


5.14. 2 X IO Read Performer Enhance Mode

"BBh" command supports 2 X IO Performance Enhance Mode which can further reduce command overhead through setting the "Continuous Read Mode" bits (M7-0) after the input 3-byte address (A23-A0). If the "Continuous Read Mode" bits (M5-4) = (1, 0), then the next 2 X IO Read command (after CS# is raised and then lowered) does not require the BBH command code.

If the "Continuous Read Mode" bits (M5-4) do not equal (1, 0), the next command requires the first BBH command code, thus returning to normal operation. A "Continuous Read Mode" Reset command can be used to reset (M5-4) before issuing normal command.

Figure 5-14 2 X IO Read Performance Enhance Mode (M5-4 = (1,0))



Note: 2 X IO Read Performance Enhance Mode, if M5-4 = 1, 0. If not using performance enhance recommend to set M5-4 ≠ 1, 0.

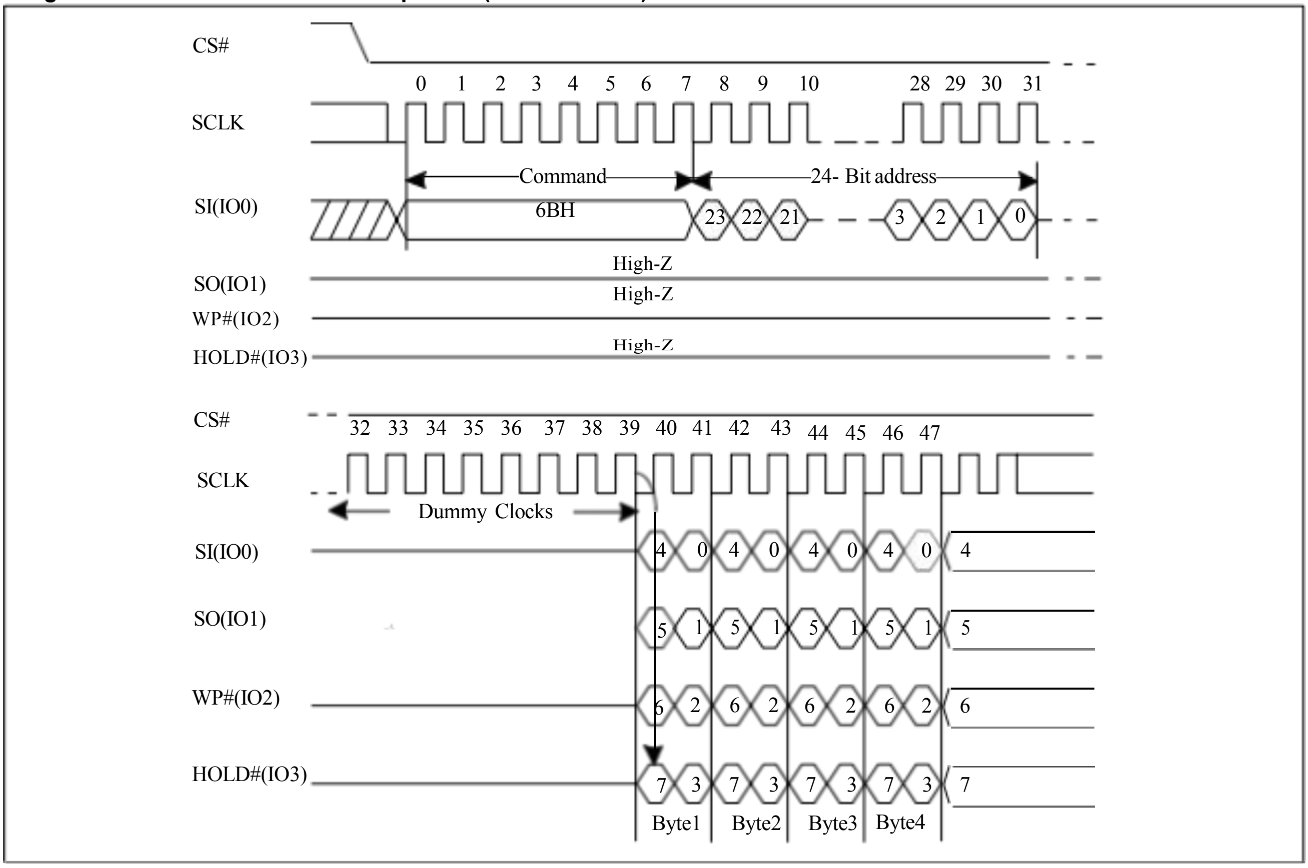
5.15. Quad Read Mode (QREAD)

The QREAD instruction enable quad throughput of Serial NOR Flash in read mode. A Quad Enable (QE) bit of status Register must be set to "1" before sending the QREAD instruction. The address is latched on rising edge of SCLK, and data of every four bits (interleave on 4 I/O pins) shift out on the falling edge of SCLK at a maximum frequency fQ. The first address byte can be at any location. The address is automatically increased to the next higher address after each byte data is shifted out, so the whole memory can be read out at a single QREAD instruction. The address counter rolls over to 0 when the highest address has been reached. Once writing QREAD instruction, the following data out will perform as 4-bit instead of previous 1-bit.

The sequence of issuing QREAD instruction is: CS# goes low→ sending QREAD instruction → 3-byte address on SI → 8-bit dummy cycle → data out interleave on SIO3, SIO2, SIO1 & SIO0→ to end QREAD operation can use CS# to high at any time during data out.

While Program/Erase/Write Status Register cycle is in progress, QREAD instruction is rejected without any impact on the Program/Erase/Write Status Register current cycle.

Figure 5-15 Quad Read Mode Sequence (Command 6B)



5.16. 4 X IO Read Mode(4READ)

The 4READ instruction enable quad throughput of Serial NOR Flash in read mode. A Quad Enable (QE) bit of status Register must be set to "1" before sending the 4READ instruction. The address is latched on rising edge of SCLK, and data of every four bits (interleave on 4 I/O pins) shift out on the falling edge of SCLK at a maximum frequency fQ. The first address byte can be at any location. The address is automatically increased to the next higher address after each byte data is shifted out, so the whole memory can be read out at a single 4READ instruction. The address counter rolls over to 0 when the highest address has been reached. Once writing 4READ instruction, the following address/dummy/data out will perform as 4-bit instead of previous 1-bit.

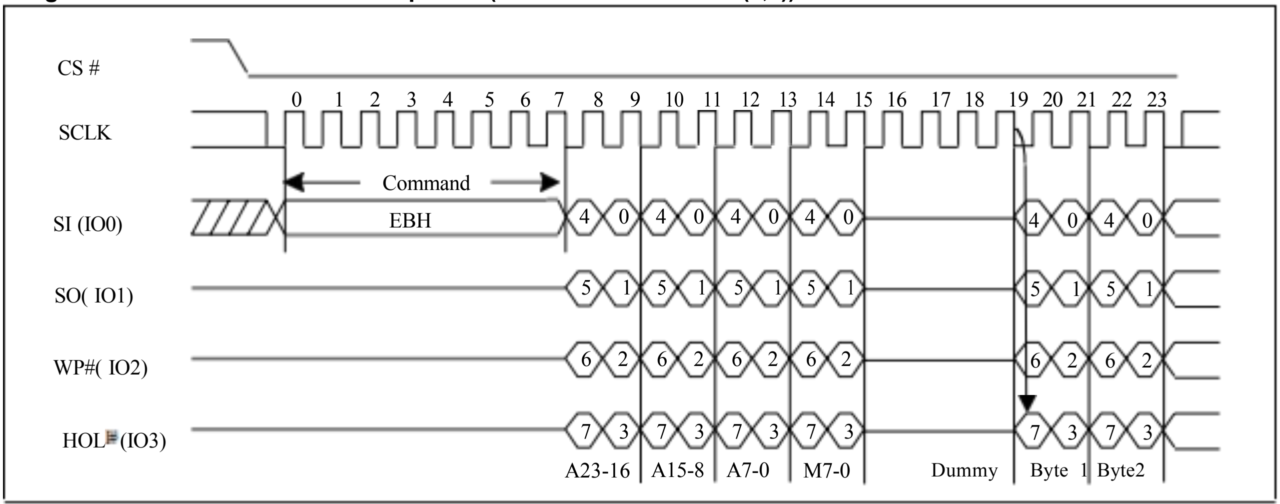
The sequence of issuing 4READ instruction is: CS# goes low→ sending 4READ instruction→ 24-bit address interleave on SIO3, SIO2, SIO1 & SIO0→2+4 dummy cycles→data out interleave on SIO3, SIO2, SIO1 & SIO0 – to end 4READ operation can use CS# to high at any time during data out.

Another sequence of issuing 4READ instruction especially useful in random access is: CS# goes low→ sending 4READ instruction→3-bytes address interleave on SIO3, SIO2, SIO1 & SIO0 → "Continuous Read Mode" byte M[7:0]→ 4 dummy cycles →data out still CS# goes high →CS# goes low(reduce4 Read instruction)
→24-bit random access address .

In the performance-enhancing mode, the "Continuous Read Mode" bits M[5:4] = (1,0) can make this mode continue and reduce the next 4READ instruction. Once M[5:4] ≠ (1,0) and afterwards CS# is raised and then lowered, the system then will escape from performance enhance mode and return to normal operation. A "Continuous Read Mode" Reset command can be used to reset (M5-4) before issuing normal command

While Program/Erase/Write Status Register cycle is in progress, 4READ instruction is rejected without any impact on the Program/Erase/Write Status Register current cycle.

Figure 5-16 4 X IO Read Mode Sequence (Command EB M5-4 ≠ (1,0))



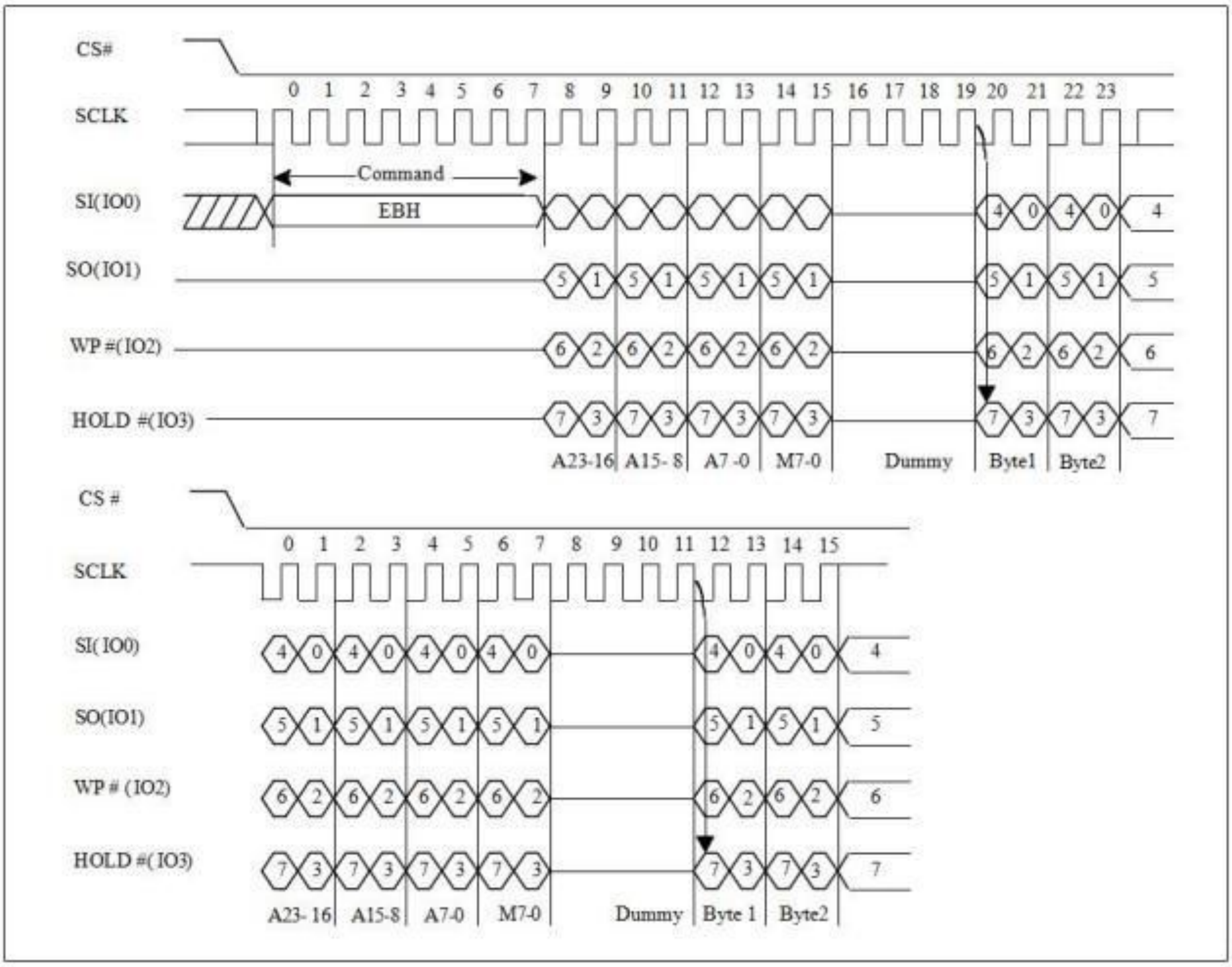
Note:
1. Hi-impedance is inhibited for the two clock cycles.
2. M[5-4] = (1,0) is inhibited.

5.17. 4 X IO Read PerformanceEnhance

"EBh" command supports 4 X IO Performance Enhance Mode which can further reduce command overhead through setting the "Continuous Read Mode" bits (M7-0) after the input 3-byte address (A23-A0). If the "Continuous Read Mode" bits (M5-4) = (1, 0), then the next 4 X IO Read command (after CS# is raised and then lowered) does not require the EBH command code.

If the "Continuous Read Mode" bits (M5-4) do not equal (1, 0), the next command requires the first EBH command code, thus returning to normal operation. A "Continuous Read Mode" Reset command can be used to reset (M5-4) before issuing normal command.

Figure 5-17 4 x I/O Read Performance Enhance Mode Sequence (M5-4 = (1,0))



Note: 1. 4 X IO Read Performance Enhance Mode, if M5-4 = 1, 0. If not using performance enhance

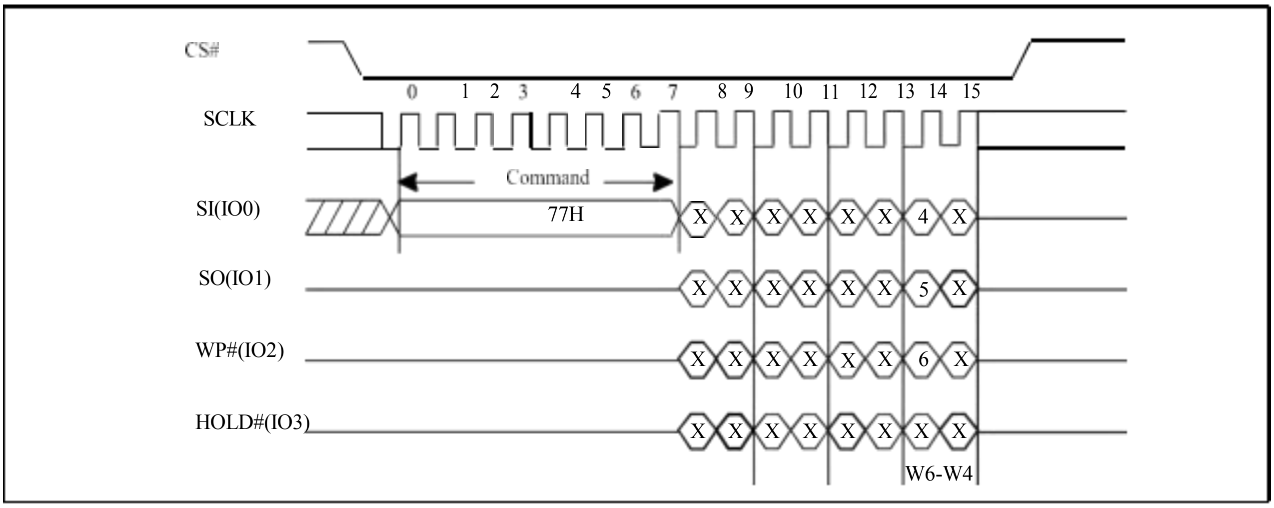
5.18. Burst Read

The Set Burst with Wrap command is used in conjunction with "4 X IO Read" command to access a fixed length of 8/16/32/64-byte section within a 256-byte page, in standard SPI mode.
The Set Burst withWrap command sequence: CS# goes low → Send Set Burst with Wrap command → Send 24 dummy bits→ Send 8 bits "Wrap bits" → CS# goes high.

W6,W5	W4=0		W4=1 (default)	
	Wrap Aroud	Wrap Length	Wrap Aroud	Wrap Length
0,0	Yes	8-byte	No	N/A
0,1	Yes	16-byte	No	N/A
1,0	Yes	32-byte	No	N/A
1,1	Yes	64-byte	No	N/A

If the W6-W4 bits are set by the Set Burst with Wrap command,all the following "4 X IO Read"command will use the W6-W4 setting to access the 8/16/32/64-byte section within any page. To exit the "Wrap Around" function and return to normal read operation,another Set Burst with Wrap command should be isscued to setW4=1.

Figure 5-18 Burst Read (SBL) Sequence (Command 77)



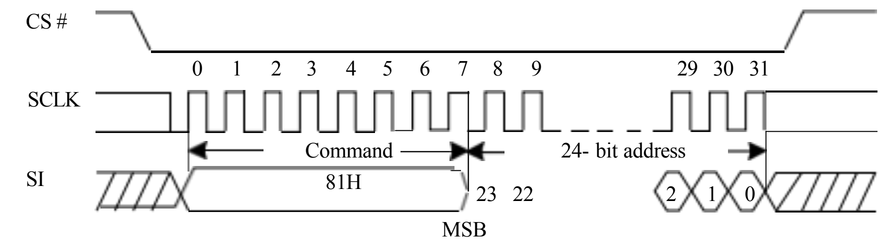
5.19. Page Erase (PE)

The Page Erase (PE) instruction is for erasing the data of the chosen Page to be "1". A Write Enable (WREN) instruction must execute to set the Write Enable Latch (WEL) bit before sending the Page Erase (PE).

To perform a Page Erase with the standard page size (256 bytes), an opcode of 81h must be clocked into the device followed by three address bytes comprised of 2 page address bytes that specify the page in the main memory to be erased, and 1 dummy byte.

The sequence of issuing PE instruction is: CS# goes low → sending PE instruction code→ 3-byte address on SI → CS# goes high

Figure 5-19 Page Erase Sequence (Command 81)



5.20. Sector Erase (SE)

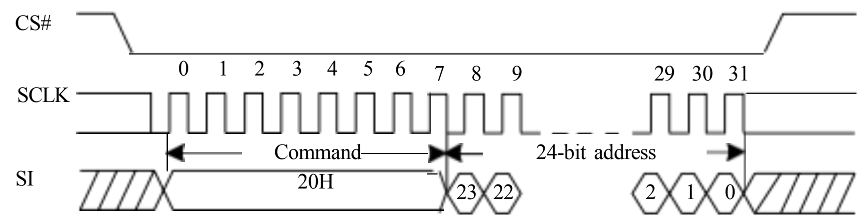
The Sector Erase (SE) instruction is for erasing the data of the chosen sector to be "1". A Write Enable (WREN) instruction must execute to set the Write Enable Latch (WEL) bit before sending the Sector Erase (SE). Any address of the sector is a valid address for Sector Erase (SE) instruction. The CS# must go high exactly at the byte boundary (the latest eighth of address byte been latched-in); otherwise, the instruction will be rejected and not executed.

Address bits [Am-A12] (Am is the most significant address) select the sector address.

The sequence of issuing SE instruction is: CS# goes low → sending SE instruction code→ 3-byte address on SI → CS# goes high.

The SIO[3:1] are don't care.

Figure 5-20 Sector Erase (SE) Sequence (Command 20)



5.21. Block Erase (BE32K)

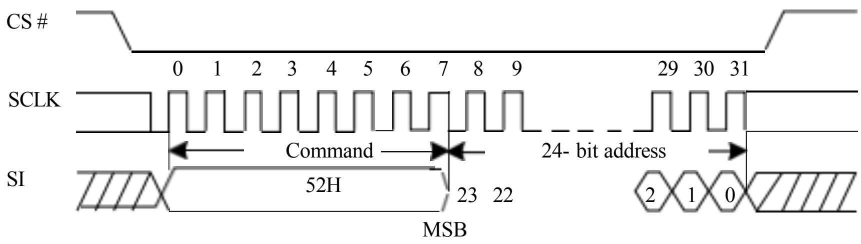
The Block Erase (BE32K) instruction is for erasing the data of the chosen block to be "1". The instruction is used for 32K-byte block erase operation. A Write Enable (WREN) instruction must be executed to set the Write Enable Latch (WEL) bit before sending the Block Erase (BE32K). Any address of the block is a valid address for Block Erase (BE32K) instruction. The CS# must go high exactly at the byte boundary (the least significant bit of address byte has been latched-in); otherwise, the instruction will be rejected and not executed.

The sequence of issuing BE32K instruction is: CS# goes low → sending BE32K instruction code → 3-byte address on SI → CS# goes high.

The SIO[3:1] are don't care.

The self-timed Block Erase Cycle time (tBE32K) is initiated as soon as Chip Select (CS#) goes high. The Write in Progress (WIP) bit still can be checked while the Block Erase cycle is in progress. The WIP sets during the tBE32K timing, and clears when Block Erase Cycle is completed, and the Write Enable Latch (WEL) bit is cleared. If the block is protected by BP4, BP3, BP2, BP1,BP0 bits, the array data will be protected (no change) and the WELbit still be reset.

Figure 5-21 Block Erase 32K(BE32K) Sequence (Command 52)



5.22. Block Erase (BE)

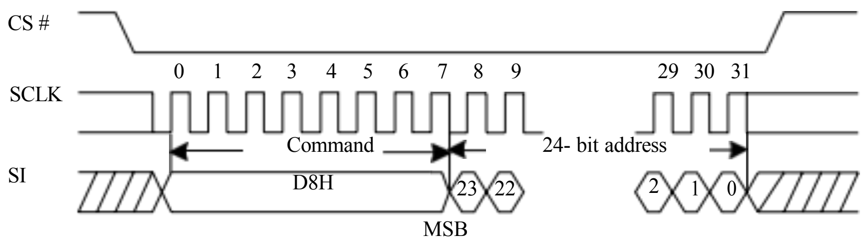
The Block Erase (BE) instruction is for erasing the data of the chosen block to be "1". The instruction is used for 64K-byte block erase operation. A Write Enable (WREN) instruction must execute to set the Write Enable Latch (WEL) bit before sending the Block Erase (BE). Any address of the block is a valid address for Block Erase (BE) instruction. The CS# must go high exactly at the byte boundary (the latest eighth of address byte been latched-in); otherwise, the instruction will be rejected and not executed.

The sequence of issuing BE instruction is: CS# goes low→ sending BE instruction code→ 3-byte address on SI→CS# goes high.

The SIO[3:1] are "don't care".

The self-timed Block Erase Cycle time (tBE) is initiated as soon as Chip Select (CS#) goes high. The Write in Progress (WIP) bit still can be checked during the Block Erase cycle is in progress. The WIP sets 1 during the tBE timing, and sets 0 when Block Erase Cycle is completed, and the Write Enable Latch (WEL) bit is reset. If the block is protected by BP4, BP3, BP2, BP1, BP0 bits, the Block Erase (BE) instruction will not be executed on the block.

Figure 5-22 Block Erase (BE) Sequence (Command D8)



5.23. Chip Erase (CE)

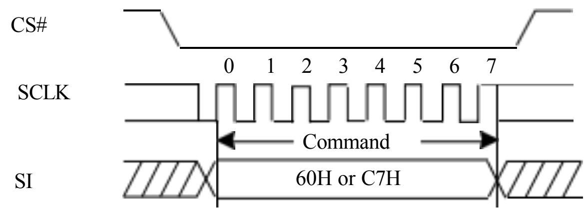
The Chip Erase (CE) instruction is for erasing the data of the whole chip to be "1". A Write Enable (WREN) instruction must execute to set the Write Enable Latch (WEL) bit before sending the Chip Erase (CE). The CS# must go high exactly at the byte boundary (the latest eighth of address byte been latched-in); otherwise, the instruction will be rejected and not executed.

The sequence of issuing CE instruction is: CS# goes low→ sending CE instruction code→ CS# goes high.

The SIO[3:1] are "don't care".

The self-timed Chip Erase Cycle time (tCE) is initiated as soon as Chip Select (CS#) goes high. The Write in Progress (WIP) bit still can be checked during the Chip Erase cycle is in progress. The WIP sets 1 during the tCE timing, and sets 0 when Chip Erase Cycle is completed, and the Write Enable Latch (WEL) bit is reset. If the chip is protected by BP4,BP3, BP2, BP1, BP0 bits, the Chip Erase (CE) instruction will not be executed. It will be only executed when all Block Protect(BP4, BP3, BP2, BP1, BP0) are set to “None protected”.

Figure 5-23 Chip Erase (CE) Sequence (Command 60 or C7)



5.24. Page Program (PP)

The Page Program (PP) instruction is for programming the memory to be "0". A Write Enable (WREN) instruction must execute to set the Write Enable Latch (WEL) bit before sending the Page Program (PP). The device programs only the last 256 data bytes sent to the device. If the entire 256 data bytes are going to be programmed, A7-A0 (The eight least significant address bits) should be set to 0. If the eight least significant address bits (A7-A0) are not all 0, all transmitted data going beyond the end of the current page are programmed from the start address of the same page (from the address A7-A0 are all 0). If more than 256 bytes are sent to the device, the data of the last 256-byte is programmed at the request page and previous data will be disregarded. If less than 256 bytes are sent to the device, the data is programmed at the requested address of the page without effect on other address of the same page.

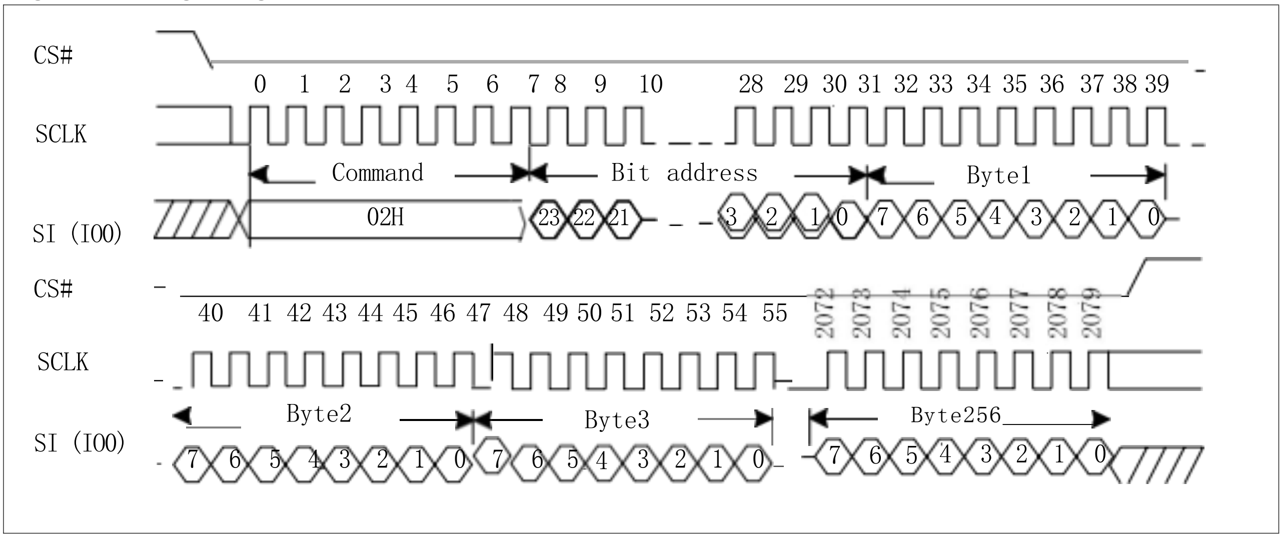
The sequence of issuing PP instruction is: CS# goes low→ sending PP instruction code→ 3-byte address on SI→ at least 1-byte on data on SI→ CS# goes high.

The CS# must be kept low during the whole Page Program cycle; The CS# must go high exactly at the byte boundary (the latest eighth bit of data being latched in), otherwise the instruction will be rejected and will not be executed.

The self-timed Page Program Cycle time (tPP) is initiated as soon as Chip Select (CS#) goes high. The Write in Progress (WIP) bit still can be checked during the Page Program cycle is in progress. The WIP sets 1 during the tPP timing, and sets 0 when Page Program Cycle is completed, and the Write Enable Latch (WEL) bit is reset. If the page is protected by BP4, BP3, BP2, BP1, BP0 bits, the Page Program (PP) instruction will not be executed.

The SIO[3:1] are "don't care".

Figure 5-24 Page Program (PP) Sequence (Command 02)



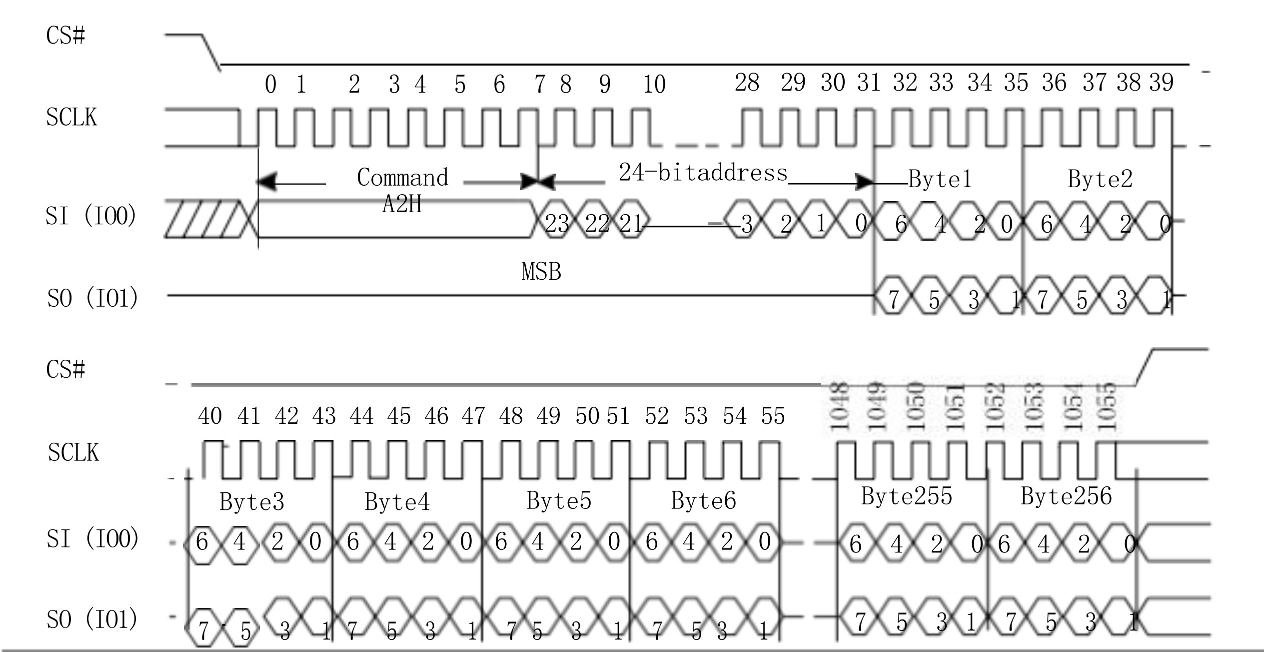
5.25. Dual Input Page Program(DPP)

The Dual Input Page Program (DPP) instruction is similar to the standard Page Program command and can be used to program anywhere from a single byte of data up to 256 bytes of data into previously erased memory locations. The Dual-Input Page Program command allows two bits of data to be clocked into the device on every clock cycle rather than justone.

A Write Enable (WREN) instruction must execute to set the Write Enable Latch (WEL) bit before sending the Dual Input Page Program (DPP). The Dual Input Page Programming takes two pins: SIO0, SIO1 as data input, which can improve programmer performance and the effectiveness of application. The other function descriptions are as same as standard page program.

The sequence of issuing DPP instruction is: CS# goes low→ sending DPP instruction code→ 3-byte address on SI→at least 1-byte on data on SIO[1:0]→ CS# goes high.

Figure 5-25 Page Program (DPP) Sequence (Command A2)

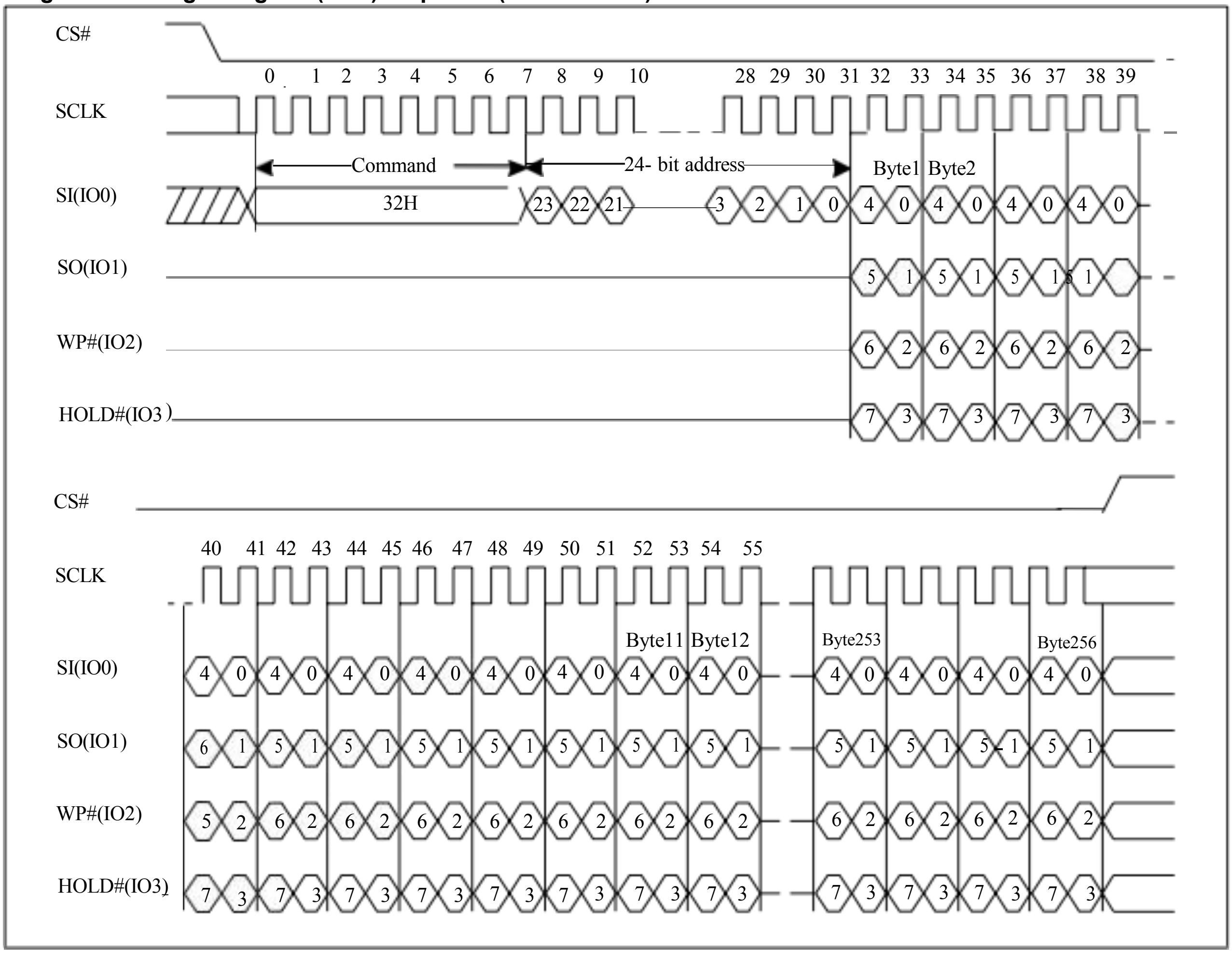


5.26. Quad Page Program (QPP)

The Quad Page Program (QPP) instruction is for programming the memory to be "0". A Write Enable (WREN) instruction must execute to set the Write Enable Latch (WEL) bit and Quad Enable (QE) bit must be set to "1" before sending the Quad Page Program (QPP). The Quad Page Programming takes four pins: SIO0, SIO1, SIO2, and SIO3 as data input, which can improve programmer performance and the effectiveness of application. The QPP operation frequency supports as fast as fQPP. The other function descriptions are as same as standard page program.

The sequence of issuing QPP instructions:CS# goes low → sending QPP instruction code→ 3-byte address on SI→at least 1-byte on data on SIO[1:0]→ CS# goes high.

Figure 5-26 Page Program (QPP) Sequence (Command 32)



5.27. Erase Security Registers (ERSCUR)

The product provides three512-byte Security Registers which can be erased and programmed individually. These registers may be used by the system manufacturers to store security and other important information separately from the main memory array.

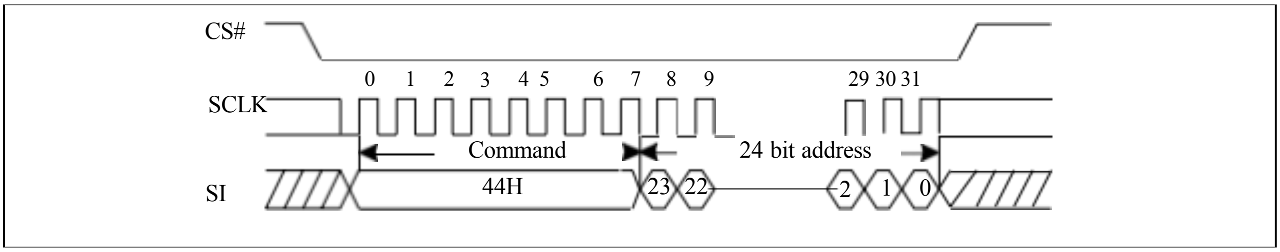
The Erase Security Registers command is similar to Sector/Block Erase command, the instruction is used for 512-byte erase operation. A Write Enable (WREN) command must previously have been executed to set the Write Enable Latch (WEL) bit.

The Erase Security Registers command sequence: CS# goes low → sending ERSCUR instruction → sending 24 bit address → CS# goes high.

CS# must be driven high after the eighth bit of the command code has been latched in; otherwise the Erase Security Registers command is not executed. As soon as CS# is driven high, the self-timed Erase Security Registers cycle (whose duration is tSE) is initiated. While the Erase Security Registers cycle is in progress, the Status Register may be read to check the value of the Write in Progress (WIP) bit. The Write in Progress (WIP) bit is 1 during the self-timed Erase Security Registers cycle, and is 0 when it is completed. The Security Registers Lock Bit (LB3-1) in the Status Register can be used to OTP protect the security registers. Once the LB bit is set to 1, the Security Registers will be permanently locked; the Erase Security Registers command will

Address	A23-16	A15-12	A11-9	A8-0
Security Register #1	00H	0001	000	Don't care
Security Register #2	00H	0010	000	Don't care
Security Register #3	00H	0011	000	Don't care

Figure 5-27 Erase Security Registers (ERSCUR) Sequence (Command 44)



5.28. Program Security Registers (PRSCUR)

The Program Security Registers command is similar to the Page Program command. It allows from 1 to 512bytes Security Registers data to be programmed. A Write Enable (WREN) command must previously have been executed to set the Write Enable Latch (WEL) bit before sending the Program Security Registers command.

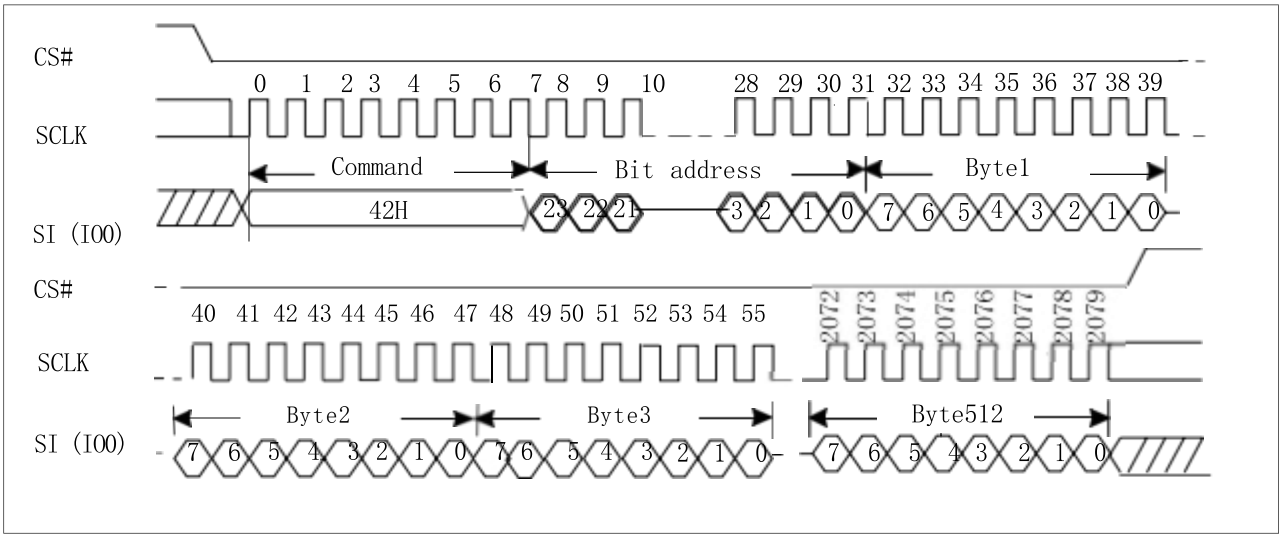
The Program Security Registers command sequence: CS# goes low → sending PRSCUR instruction → sending 24 bit address → sending at least one byte data → CS# goes high.

As soon as CS# is driven high, the self-timed Program Security Registers cycle (whose duration is tPP) is initiated. While the Program Security Registers cycle is in progress, the Status Register may be read to check the value of the Write in Progress (WIP) bit. The Write in Progress (WIP) bit is 1 during the self-timed Program Security Registers cycle, and is 0 when it is completed.

If the Security Registers Lock Bit (LB3-1) is set to 1, the Security Registers will be permanently locked. Program Security Registers command will be ignored.

Address	A23-16	A15-12	A5-9	A8-0
Security Register #1	00H	0001	000	Byte Address
Security Register #2	00H	0010	000	Byte Address
Security Register #3	00H	0011	000	Byte Address

Figure 5-28 Program Security Registers (PRSCUR) Sequence (Command 42)



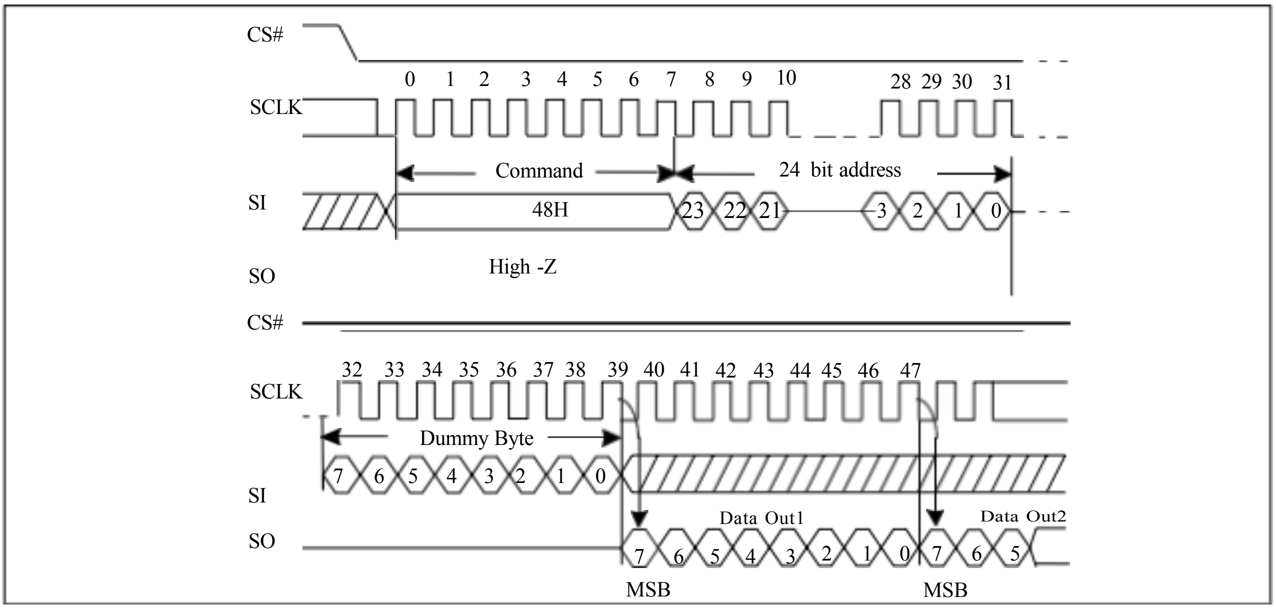
5.29. Read Security Registers (RDSCUR)

The Read Security Registers command is similar to Fast Read command. The command is followed by a 3-byte address (A23-A0) and a dummy byte, each bit being latched-in during the rising edge of SCLK. Then the memory content, at that address, is shifted out on SO, each bit being shifted out, at a Max frequency fC, during the falling edge of SCLK. The first byte addressed can be at any location. The address is automatically incremented to the next higher address after each byte of data is shifted out. Once the A8-A0 address reaches the last byte of the register (Byte 1FFH), it will reset to 000H, the command is completed by driving CS# high.

The sequence of issuing RDSCUR instruction is : CS# goes low → sending RDSCUR instruction → sending 24 bit address → 8 bit dummy byte → Security Register data out on SO → CS# goes high.

Address	A23-16	A15-12	A5-9	A8-0
Security Register #1	00H	0001	000	Byte Address
Security Register #2	00H	0010	000	Byte Address
Security Register #3	00H	0011	000	Byte Address

Figure 5-29 Read Security Registers (RDSCUR) Sequence (Command 48)



5.30. Deep Power-down (DP)

The Deep Power-down (DP) instruction is for setting the device on the minimizing the power consumption (to entering the Deep Power-down mode), the standby current is reduced from ISB1 to ISB2). The Deep

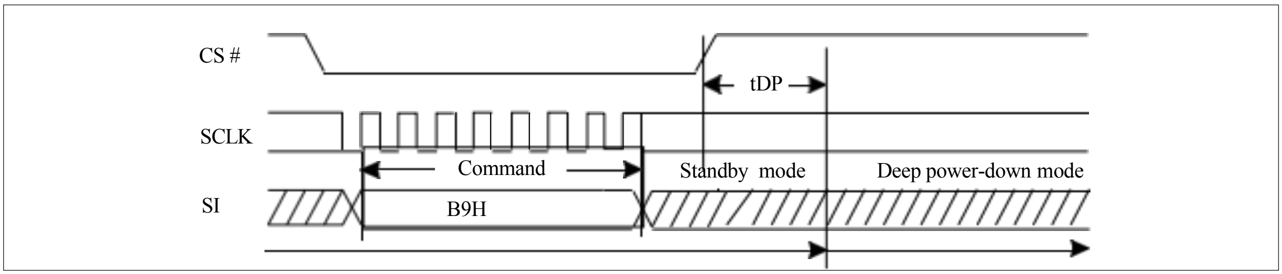
Power-down mode requires the Deep Power-down (DP) instruction to enter, during the Deep Power-down mode, the device is not active and all Write/Program/Erase instruction are ignored. When CS# goes high, it's only in standby mode not deep power-down mode. It's different from Standby mode.

The sequence of issuing DP instruction is: CS# goes low→ sending DP instruction code→ CS# goes high.

Once the DP instruction is set, all instruction will be ignored except the Release from Deep Power-down mode (RDP) and Read Electronic Signature (RES) instruction. (RES instruction to allow the ID been read out).

When Power- down, the deep power-down mode automatically stops, and when power-up, the device automatically is in standby mode. For RDP instruction the CS# musOnce the DP instruction is set, all instruction will be ignored except the Release from Deep Power-down mode (RDP) and Read Electronic Signature (RES) instruction. (RES instruction to allow the ID been read out).
t go high exactly at the byte boundary (the latest eighth bit of instruction code been latched-in); otherwise, the instruction will not be executed. As soon as Chip Select (CS#) goes high, a delay of tDP is required before entering the Deep Power-down mode and reducing the current to ISB2.

Figure 5-30 Deep Power-down (DP) Sequence (Command B9)



5.31. Release form Deep Power-Down (RDP), Read Electronic Signature (RES)

The Release from Deep Power-down (RDP) instruction is terminated by driving Chip Select (CS#) High. When Chip Select (CS#) is driven high, the device is put in the Stand-by Power mode. If the device was not previously in the Deep Power-down mode, the transition to the Stand-by Power mode is immediate. If the device was previously in the Deep Power-down mode, though, the transition to the Stand-by Power mode is delayed by tRES2, and Chip Select (CS#) must remain High for at least tRES2(max). Once in the

Stand-by Power mode, the device waits to be selected, so that it can receive, decode and execute instructions.

RES instruction is for reading out the old style of 8-bit Electronic Signature, whose values are shown as table of ID Definitions. This is not the same as RDID instruction. It is not recommended to use for new design. For new design, please use RDID instruction.Even in Deep power-down mode, the RDP and RES are also allowed to be executed, only except the device is in progress of program/erase/write cycle; there's no effect on the current program/erase/ write cycle in progress.

The RES instruction is ended by CS# goes high after the ID been read out at least once. The ID outputs repeatedly if continuously send the additional clock cycles on SCLK while CS# is at low. If the device was not previously in Deep Power-down mode, the device transition to standby mode is immediate. If the device was previously in Deep Power-down mode, there's a delay of tRES2 to transit to standby mode, and CS# must remain to high at least tRES2 (max). Once in the standby mode, the device waits to be selected, so it can be receive, decode, and execute instruction.

The RDP instruction is for releasing from Deep Power-Down Mode.

Figure 5-31 Read Electronic Signature (RES) Sequence (Command AB)

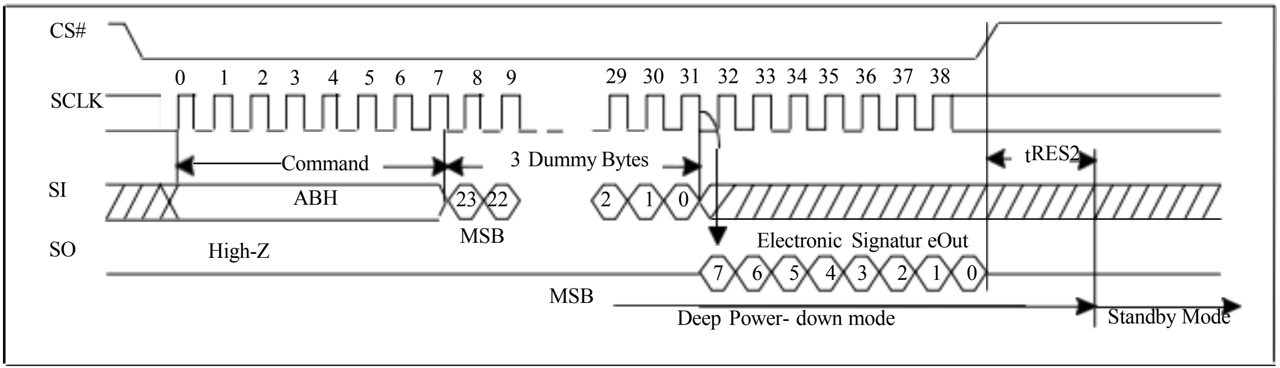
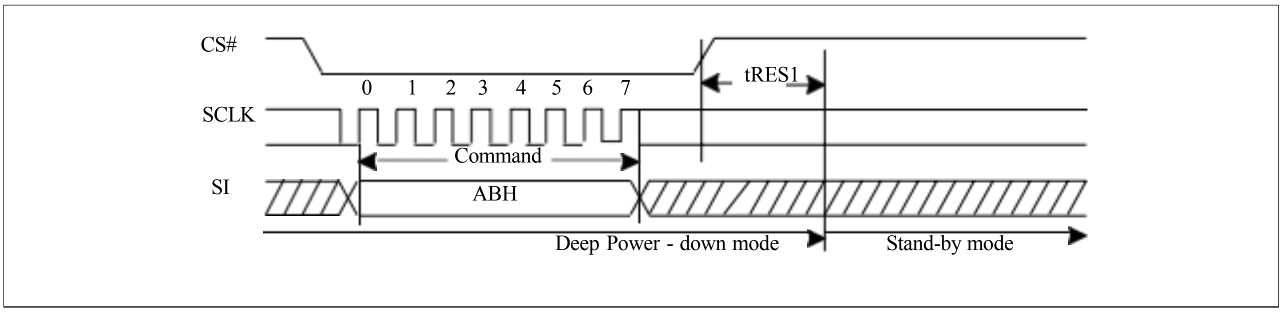


Figure 5-32 Release from Deep Power-down (RDP) Sequence (Command AB)

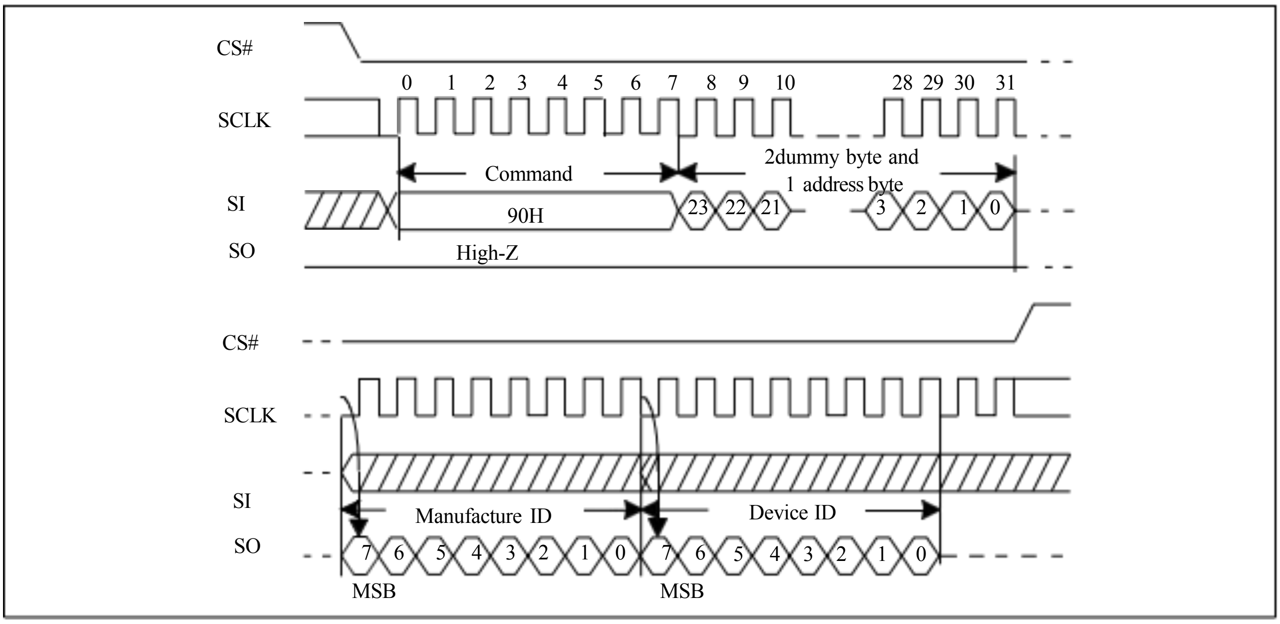


5.32. Read Electronic Manufacturer ID & Device ID (REMS)

The REMS instruction returns both the JEDEC assigned manufacturer ID and the device ID. The Device ID values are listed in "Table ID Definitions".

The REMS instruction is initiated by driving the CS# pin low and sending the instruction code "90h" followed by two dummy bytes and one address byte (A7~A0). After which the manufacturer ID for Along and the device ID are shifted out on the falling edge of SCLK with the most significant bit (MSB) first. If the least significant bit (LSB) of the address byte is 0b, the manufacturer ID will be output first, followed by the device ID. If the least significant bit (LSB) of the address byte is 1b, then the device ID will be output first, followed by the manufacturer ID. While CS# is low, the manufacturer and device IDs can be read continuously, alternating from one to the other. The instruction is completed by driving CS# high.

Figure 5-32 Read Electronic Manufacturer & Device ID (REMS) Sequence (Command 90)

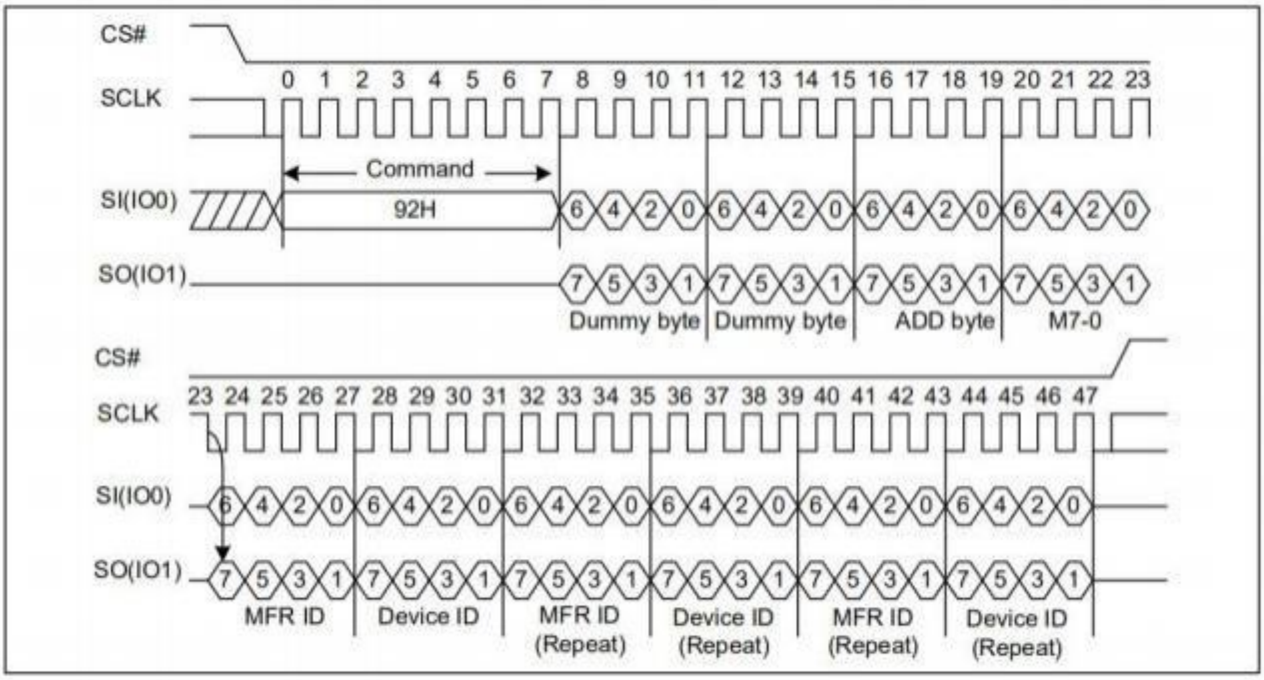


5.33. Dual I/O Read Electronic Manufacturer ID & Device ID (DREMS)

The DREMS instruction is similar to the REMS command and returns the JEDEC assigned manufacturer ID which takes two pins: SIO0, SIO1 as address input and ID output I/O

The instruction is initiated by driving the CS# pin low and shift the instruction code "92h" followed by two dummy bytes and one bytes address (A7~A0). After which, the Manufacturer ID for Along and the Device ID are shifted out on the falling edge of SCLK with most significant bit (MSB) first. If the least significant bit (LSB) of the one-byte address is initially set to 1b, then the device ID will be read first and then followed by the Manufacturer ID. The Manufacturer and Device IDs can be read continuously, alternating from one to the other. The instruction is completed by driving CS# high.

Figure 5-33 DUAL I/O Read Electronic Manufacturer & Device ID (DREMS) Sequence (Command 92)

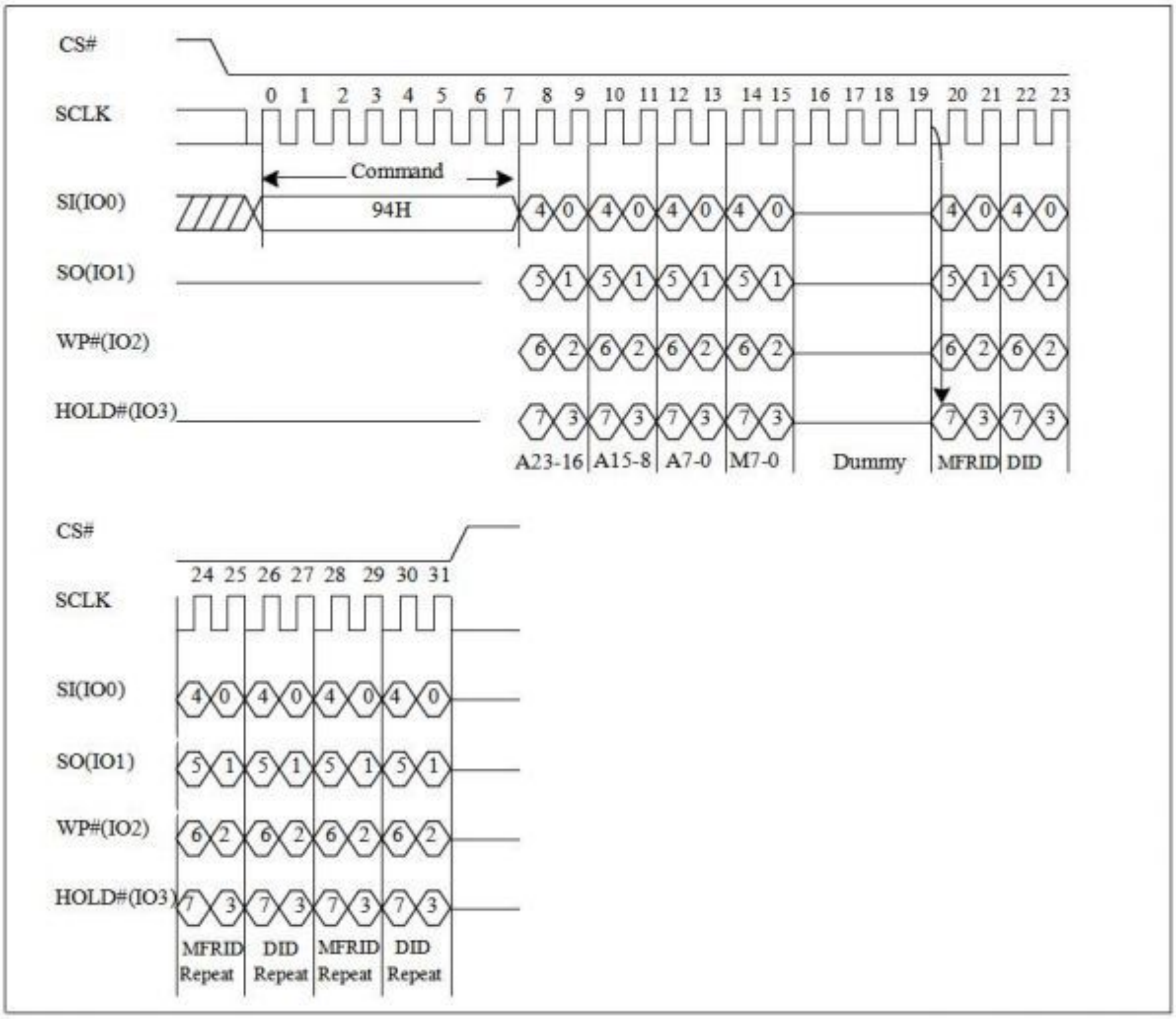


5.34. Quad I/O Read Electronic Manufacturer ID & Device ID (QREMS)

The QREMS instruction is similar to the REMS command and returns the JEDEC assigned manufacturer ID which takes four pins: SIO0, SIO1,SIO2,SIO3 as address input and ID output I/O

The instruction is initiated by driving the CS# pin low and shift the instruction code "94h" followed by two dummy bytes and one bytes address (A7~A0). After which, the Manufacturer ID for Along and the Device ID are shifted out on the falling edge of SCLK with most significant bit (MSB) first. If the least significant bit (LSB) of the one-byte address is initially set to 1b, then the device ID will be read first and then followed by the Manufacturer ID. The Manufacturer and Device IDs can be read continuously, alternating from one to the other. The instruction is completed by driving CS# high.

Figure 5-34 QUAD I/O Read Electronic Manufacturer & Device ID (QREMS) Sequence (Command 94)



5.35. Read Identification (RDID)

The RDID instruction is for reading the manufacturer ID of 1-byte and followed by Device ID of 2-byte. The Along Manufacturer ID and Device ID are list as “as "Table . ID Definitions”.

The sequence of issuing RDID instruction is: CS# goes low→ sending RDID instruction code →24-bits ID data out on SO→ to end RDID operation can use CS# to high at any time during data out.

While Program/Erase operation is in progress, it will not decode the RDID instruction, so there's no effect on the cycle of program/erase operation which is currently in progress. When CS# goes high, the device is at standby stage.

Figure 5-35 Read Identification(RDID) Sequence (Command 9F)

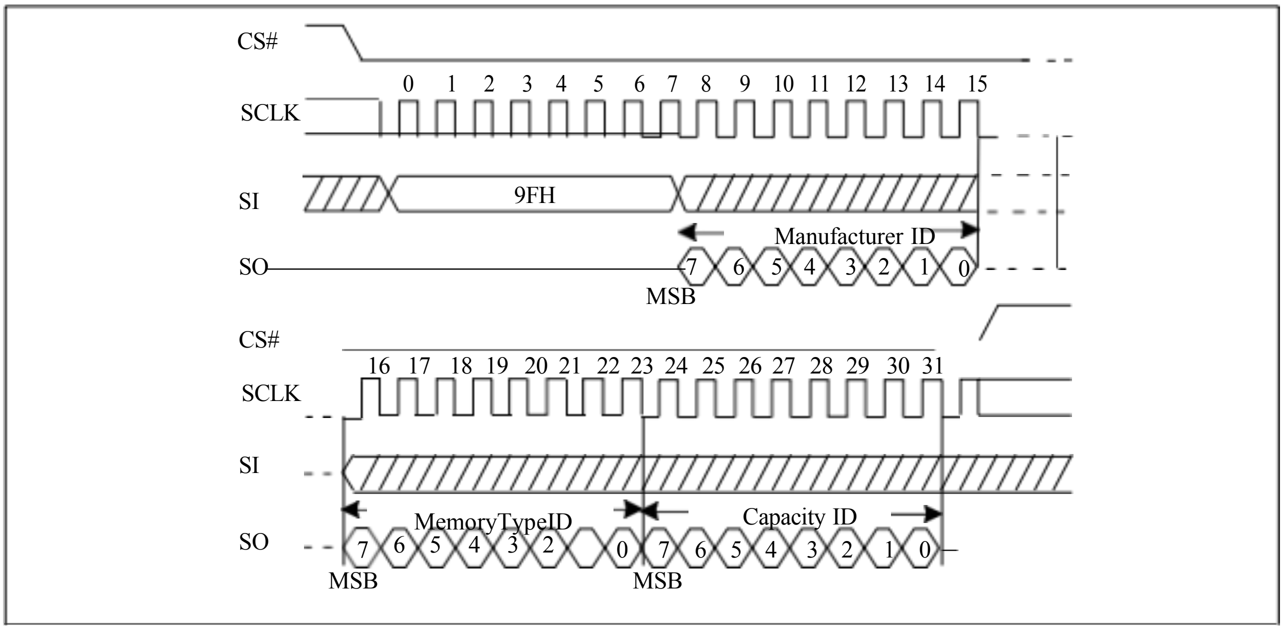


Table ID Definitions

AL25WQ80	RDID command	manufacturer ID	memory type	memory density
		BA	60	14
	RES command	electronic ID		
		13		
	REMS command	manufacturer ID		device ID
		BA		13

5.36. Program/Erase Suspend/Resume

The Suspend instruction interrupts a Page Program, Sector Erase, or Block Erase operation to allow access to the memory array. After the program or erase operation has entered the suspended state, the memory array can be read except for the page being programmed or the sector or block being erased.

Readable Area of Memory While a Program or Erase Operation is Suspended

Suspended Operation	Readable Region of Memory Array
Page Program	All but the Page being programmed
Page Erase	All but the Page being erased
Sector Erase(4KB)	All but the 4KB Sector being erased
Block Erase(32KB)	All but the 32KB Block being erased
Block Erase(64KB)	All but the 64KB Block being erased

When the Serial NOR Flash receives the Suspend instruction, there is a latency of tPSL or tESL before the Write Enable Latch (WEL) bit clears to “0” and the SUS2 or SUS1 sets to “1”, after which the device is ready to accept one of the commands listed in "Table Acceptable Commands During Program/Erase Suspend after tPSL/tESL" (e.g. FAST READ). Refer to " AC Characteristics" for tPSL and tESL timings. "Table Acceptable Commands During Suspend (tPSL/tESL not required)" lists the commands for which the tPSL and tESL latencies do not apply. For example, RDSR, RDSCUR, RSTEN, and RST can be issued at any time after the Suspend instruction.

Status Register bit 15 (SUS2) and bit 10 (SUS1) can be read to check the suspend status. The SUS2 (Program Suspend Bit) sets to “1” when a program operation is suspended. The SUS1 (Erase Suspend Bit) sets to “1” when an erase operation is suspended. The SUS2 or SUS1 clears to “0” when the program or erase operation is resumed.

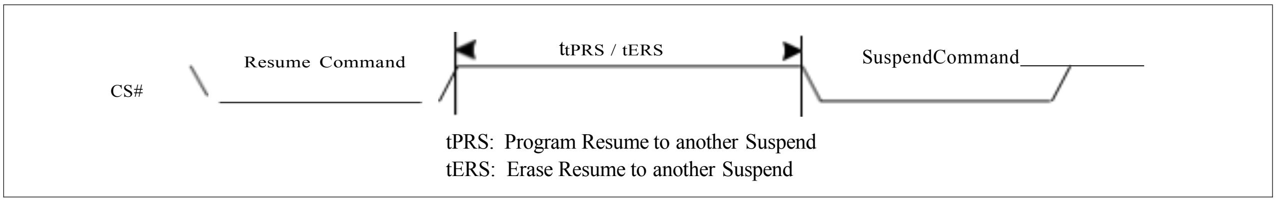
Acceptable Commands During Program/Erase Suspend after tPSL/tESL

Command name	Command Code	Suspend Type	
		Program Suspend	Erase Suspend
READ	03H		
FAST READ	0BH		
DREAD	3BH		
QREAD	6BH		
2READ	BBH		
4READ	EBH		
RDSFDP	5AH		
RDID	9FH		
REMS	90H		
DREMS	92H		
QREMS	94H		
RDSCUR	48H		
SBL	77H		
WREN	06H		
RESUME	7AH OR 30H		
PP	02H		
DPP	A2H		
QPP	32H		

Acceptable Commands During Suspend（tPSL/tESL not required）

Command name	Command Code	Suspend Type	
		Program Suspend	Erase Suspend
WRDI	04H	•	•
RDSR	05H	•	•
RDSR2	35H	•	•
ASI	25H	•	•
RES	ABH	•	•
RSTEN	66H	•	•
RST	99H	•	•
NOP	00H	•	•

Figure 5-36 Resume to Suspend Latency

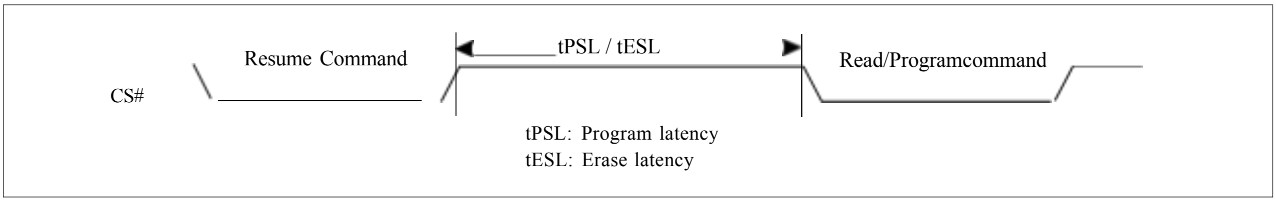


5.37. Erase Suspend to Program

The "Erase Suspend to Program" feature allows Page Programming while an erase operation is suspended. Page Programming is permitted in any unprotected memory except within the sector of a suspended Sector Erase operation or within the block of a suspended Block Erase operation. The Write Enable (WREN) instruction must be issued before any Page Program instruction.

A Page Program operation initiated within a suspended erase cannot itself be suspended and must be allowed to finish before the suspended erase can be resumed. The Status Register can be polled to determine the status of the Page Program operation. The WEL and WIP bits of the Status Register will remain "1" while the Page Program operation is in progress and will both clear to "0" when the Page Program operation completes.

Figure 5-37 Suspend to Read/Program Latency



Notes:

1. Please note that Program only available after the Erase-Suspend operation
2. To check suspend ready information, please read status register bit15 (SUS2) and bit10(SUS1)

5.38. Program Resume and EraseResume

The Resume instruction resumes a suspended Page Program, Sector Erase, or Block Erase operation. Before issuing the Resume instruction to restart a suspended erase operation, make sure that there is no Page Program operation in progress.

Immediately after the Serial NOR Flash receives the Resume instruction, the WEL and WIP bits are set to "1" and the SUS2 or SUS1 is cleared to "0". The program or erase operation will continue until finished ("Resume to Read Latency") or until another Suspend instruction is received. A resume-to-suspend latency of tPRS or tERS must be observed before issuing another Suspend instruction ("Resume to Suspend Latency").

Figure 5-38 Resume to Read Latency

5.39. No Operation (NOP)

The "No Operation" command is only able to terminate the Reset Enable (RSTEN) command and will not affect any other command.

The SIO[3:1] are don't care.

5.40. Software Reset (RSTEN/RST)

The Software Reset operation combines two instructions: Reset-Enable (RSTEN) command and Reset (RST) command. It returns the device to a standby mode. All the volatile bits and settings will be cleared then, which makes the device return to the default status as power on.

To execute Reset command (RST), the Reset-Enable (RSTEN) command must be executed first to perform the Reset operation. If there is any other command to interrupt after the Reset-Enable command, the

Reset-Enable will be invalid. The SIO[3:1] are "don't care".

If the Reset command is executed during program or erase operation, the operation will be disabled, the data under processing could be damaged orlost.

Figure 5-40a Software Reset

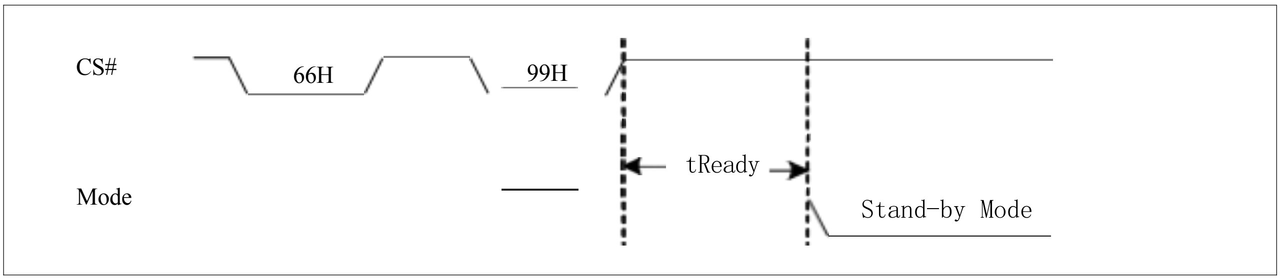
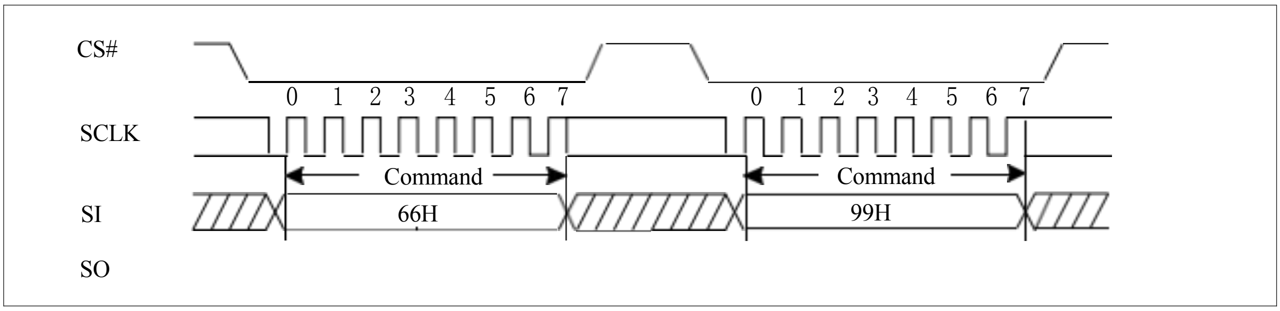


Figure 5-40b Reset



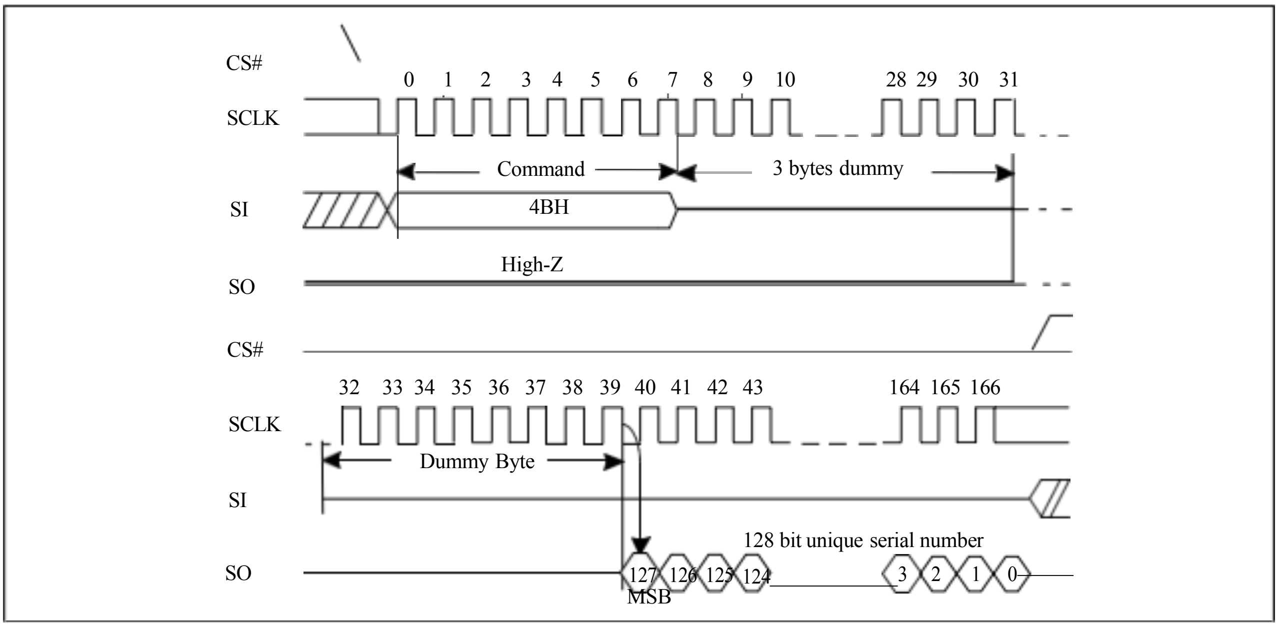
5.41. Read Unique ID (RUID)

The Read Unique ID command accesses a factory-set read-only 128bit number that is unique to each AL25Qxx device. The Unique ID can be used in conjunction with user software methods to help prevent copying or cloning of a system.

The Read Unique ID command sequence: CS# goes low → sending Read Unique ID command →Dummy Byte1 →Dummy Byte2 →Dummy Byte3 → Dummy Byte4 → 128bit Unique ID Out → CS# goes high.

The command sequence is show below.

Figure 5-41 Read Unique ID (RUID) Sequence (Command 4B)



5.42. Read SFDP Mode (RDSFDP)

The Serial Flash Discoverable Parameter (SFDP) standard provides a consistent method of describing the functional and feature capabilities of serial flash devices in a standard set of internal parameter tables. These parameter tables can be interrogated by host system software to enable adjustments needed to accommodate divergent features from multiple vendors. The concept is similar to the one found in the Introduction of JEDEC Standard, JESD68 on CFI.

The sequence of issuing RDSFDP instruction is same as FAST_READ: CS# goes low→ send RDSFDP instruction (5Ah)→send 3 address bytes on SI pin→ send 1 dummy byte on SI pin→ read SFDP code on SO→ to end RDSFDP operation can use CS# to high at any time during data out. The lower byte (A7~A0) of the address is the valid address which is corresponded to the Add in the **Figure 5-42.**

SFDP is a JEDEC Standard, JESD216B.

Figure 5-42 Read Serial Flash Discoverable Parameter(RDSFDP) Sequence

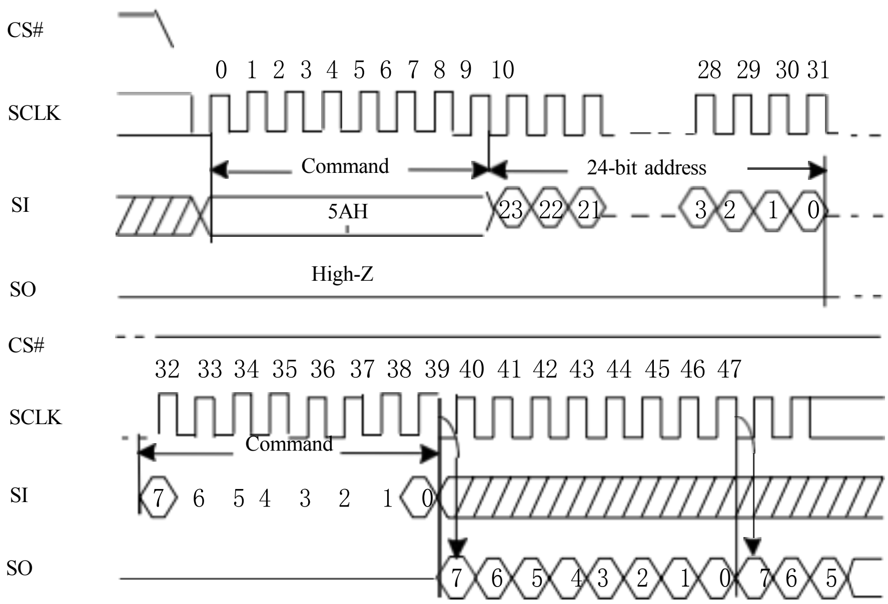


Figure 5-42 Serial Flash Discoverable Parameter (SFDP) Table

Table Signature and Parameter Identification Data Values

Description	Comment	Add(H) (Byte)	DW Add (Bit)	Data	Data
SFDP Signature	Fixed:50444653H	00H	07:00	53H	53H
		01H	15:08	46H	46H
		02H	23:16	44H	44H
		03H	31:24	50H	50H
SFDP Minor Revision Number	Start from 00H	04H	07:00	00H	00H
SFDP Major Revision Number	Start from 01H	05H	15:08	01H	01H
Number ofParameters Headers	Start from 00H	06H	23:16	01H	01H
Unused	Contains 0xFFH and can never be changed	07H	31:24	FFH	FFH
ID number (JEDEC)	00H: It indicates a JEDEC specified header	08H	07:00	00H	00H
Parameter Table Minor Revision Number	Start from 0x00H	09H	15:08	00H	00H
Parameter Table Major Revision Number	Start from 0x01H	0AH	23:16	01H	01H
Parameter Table Length (in double word)	How many DWORDs in the Parameter table	0BH	31:24	09H	09H
Parameter Table Pointer (PTP)	First address ofJEDEC Flash Parameter table	0CH	07:00	30H	30H
		0DH	15:08	00H	00H
		0EH	23:16	00H	00H
Unused	Contains 0xFFH and can never be changed	0FH	31:24	FFH	FFH
ID Number (Along Device Manufacturer ID)	It is indicates Along manufacturer ID	10H	07:00	BAH	BAH
Parameter Table Minor Revision Number	Start from 0x00H	11H	15:08	00H	00H
Parameter Table Major Revision Number	Start from 0x01H	12H	23:16	01H	01H
Parameter Table Length (in double word)	How many DWORDs in the Parameter table	13H	31:24	03H	03H
Parameter Table Pointer (PTP)	First address ofAlong Flash Parameter table	14H	07:00	60H	60H
		15H	15:08	00H	00H
		16H	23:16	00H	00H
Unused	Contains 0xFFH and can never be changed	17H	31:24	FFH	FFH

Table Parameter Table (0): JEDEC Flash Parameter Tables

Description	Comment	Add(H) (Byte)	DW Add (Bit)	Data	Data
Block/Sector Erase Size	00: Reserved; 01: 4KB erase; 10: Reserved; 11: not support 4KB erase	30H	01:00	01b	E5H
Write Granularity	0: 1Byte, 1: 64Byte or larger		02	1b	
Write Enable Instruction Requested for Writing to Volatile Status Registers	0: Nonvolatile status bit 1: Volatile status bit (BP status register bit)		03	0b	
Write Enable Opcode Select for Writing to Volatile Status Registers	0: Use 50H Opcode, 1: Use 06H Opcode, Note: Iftarget flash status register is Nonvolatile, then bits3 and 4 must be set to 00b.		04	0b	
Unused	Contains 111b and can never be changed		07:05	111b	
4KB Erase Opcode		31H	15:08	20H	20H
(1-1- 2) Fast Read	0=Not support, 1=Support	32H	16	1b	F1H
Address Bytes Number used in addressing flash array	00: 3Byte only, 01: 3 or 4Byte, 10: 4Byte only, 11: Reserved		18:17	00b	
Double Transfer Rate (DTR) clocking	0=Not support, 1=Support		19	0b	
(1-2- 2) FastRead	0=Not support, 1=Support		20	1b	
(1-4- 4) Fast Read	0=Not support, 1=Support		21	1b	
(1-1- 4) Fast Read	0=Not support, 1=Support		22	1b	
Unused			23	1b	
Unused		33H	31:24	FFH	FFH
Flash Memory Density		37H:34H	31:00	003FFFFFH	
(1-4- 4) Fast Read Number ofWait states	0 0000b: Wait states (Dummy Clocks) not support	38H	04:00	00100b	44H
(1-4- 4) Fast Read Number of Mode Bits	000b:Mode Bits not support		07:05	010b	
(1-4- 4) Fast Read Opcode		39H	15:08	EBH	EBH
(1-1- 4) Fast Read Number ofWait states	0 0000b: Wait states (Dummy Clocks) not support	3AH	20:16	01000b	08H
(1- 1- 4) Fast Read Number of Mode Bits	000b:Mode Bits not support		23:21	000b	
(1- 1- 4) Fast Read Opcode		3BH	31:24	6BH	6BH

Description	Comment	Add(H) (Byte)	DW Add (Bit)	Data	Data
(1- 1- 2) Fast Read Number ofWait states	0 0000b: Wait states (Dummy Clocks) not support	3CH	04:00	01000b	08H
(1- 1- 2) Fast Read Number ofMode Bits	000b: Mode Bits not support		07:05	000b	
(1- 1- 2) Fast Read Opcode		3DH	15:08	3BH	3BH
(1-2- 2) Fast Read Number ofWait states	0 0000b: Wait states (Dummy Clocks) not support	3EH	20:16	00000b	80H
(1-2- 2) Fast Read Number ofMode Bits	000b: Mode Bits not support		23:21	100b	
(1-2- 2) Fast Read Opcode		3FH	31:24	BBH	BBH
(2-2- 2) Fast Read	0=not support 1=support	40H	00	0b	EEH
Unused			03:01	111b	
(4-4- 4) Fast Read	0=not support 1=support		04	0b	
Unused			07:05	111b	
Unused		43H:41H	31:08	0xFFH	0xFFH
Unused		45H:44H	15:00	0xFFH	0xFFH
(2-2- 2) Fast Read Number ofWait states	0 0000b: Wait states (Dummy Clocks) not support	46H	20:16	00000b	00H
(2-2- 2) Fast Read Number ofMode Bits	000b: Mode Bits not support		23:21	000b	
(2-2- 2) Fast Read Opcode		47H	31:24	FFH	FFH
Unused		49H:48H	15:00	0xFFH	0xFFH
(4-4- 4) Fast Read Number ofWait states	0 0000b: Wait states (Dummy Clocks) not support	4AH	20:16	00000b	00H
(4-4- 4) Fast Read Number ofMode Bits	000b: Mode Bits not support		23:21	000b	
(4-4- 4) Fast Read Opcode		4BH	31:24	FFH	FFH
Sector Type 1 Size	Sector/block size=2^N bytes 0x00b: this sector type don ’ t exist	4CH	07:00	0CH	0CH
Sector Type 1 erase Opcode		4DH	15:08	20H	20H
Sector Type 2 Size	Sector/block size=2^N bytes 0x00b: this sector type don ’ t exist	4EH	23:16	0FH	0FH
Sector Type 2 erase Opcode		4FH	31:24	52H	52H
Sector Type 3 Size	Sector/block size=2^N bytes 0x00b: this sector type don ’ t exist	50H	07:00	10H	10H
Sector Type 3 erase Opcode		51H	15:08	D8H	D8H
Sector Type 4 Size	Sector/block size=2^N bytes 0x00b: this sector type don ’ t exist	52H	23:16	08H	08H
Sector Type 4 erase Opcode		53H	31:24	81H	81H

Table Parameter Table (1): Along Flash Parameter Tables

Description	Comment	Add(H) (Byte)	DW Add (Bit)	Data	Data
Vcc Supply Maximum Voltage	2000H=2.000V 2700H=2.700V 3600H=3.600V	91H:90H	15:00	3600H	3600H
Vcc Supply Minimum Voltage	1650H=1.650V 2250H=2.250V 2350H=2.350V 2700H=2.700V	93H:92H	31:16	1650H	1650H
HW Reset# pin	0=not support 1=support	95H:94H	00	0b	F99EH
HW Hold# pin	0=not support 1=support		01	1b	
Deep Power Down Mode	0=not support 1=support		02	1b	
SW Reset	0=not support 1=support		03	1b	
SW Reset Opcode	Should be issue Reset Enable(66H) before Reset cmd.		11:04	1001 1001b (99H)	
Program Suspend/Resume	0=not support 1=support		12	1b	
Erase Suspend/Resume	0=not support 1=support		13	1b	
Unused			14	1b	
Wrap Around Read mode	0=not support 1=support		15	1b	
Wrap - Around Read mode Opcode		96H	23:16	77H	77H
Wrap - Around Read data length	08H:support 8B wra-paround read 16H:8B&16B 32H:8B&16B&32B 64H:8B&16B&32B&64B	97H	31:24	64H	64H
Individualblock lock	0=not support 1=support	9BH:98H	00	0b	CBFCH
Individual block lock bit (Volatile/Nonvolatile)	0=Volatile 1=Nonvolatile		01	0b	
Individual block lock Opcode			09:02	FFH	
Individual blocklock Volatile protect bit default protect status	0=protect 1=unprotect		10	0b	
Secured OTP	0=not support 1=support		11	1b	
Read Lock	0=not support 1=support		12	0b	
Permanent Lock	0=not support 1=support		13	0b	
Unused			15:14	11b	
Unused			31:16	FFFFH	FFFFH

6. Ordering Information

AL 25XX XX X X

Company Designator
AL:ALONG

Product serial

25WD: 1.65~3.6V Dual SPI NOR
25WQ: 1.65~3.6V Quad SPI NOR

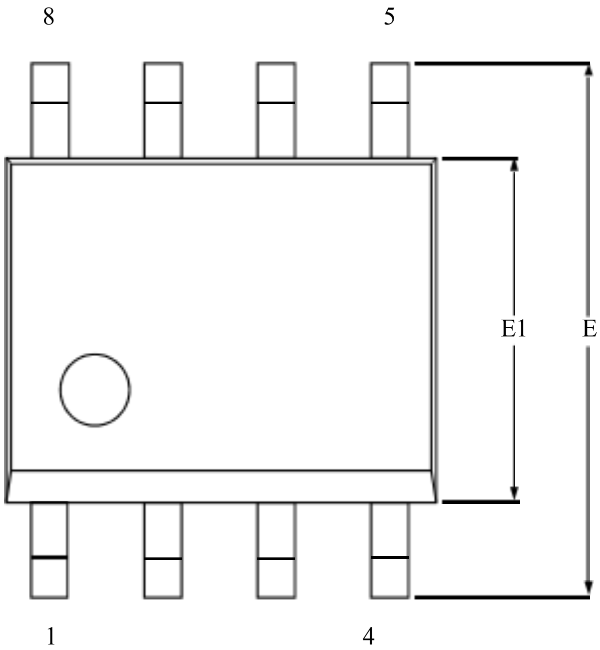
Memory desity
20:2Mbit
40:4Mbit
80:8Mbit
16:16Mbit

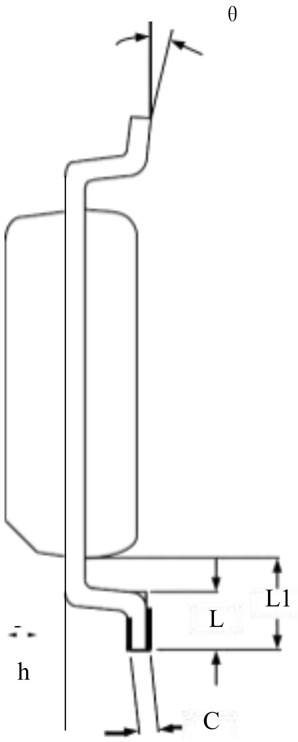
Package type
T:150mil SOP8
O:173mil TSSOP8
U:USON8 (3*2mm)

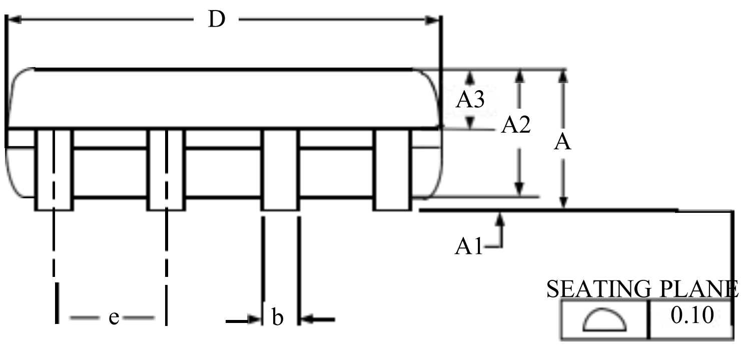
Temperature Range
I:Industrial(-40℃~85℃)
E:Extended(-25℃~85℃)

7. Package Information

7.1-Lead SOP(150mil)





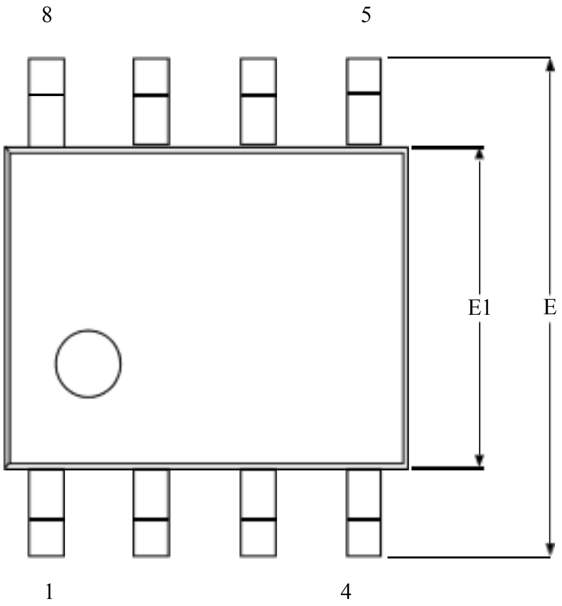


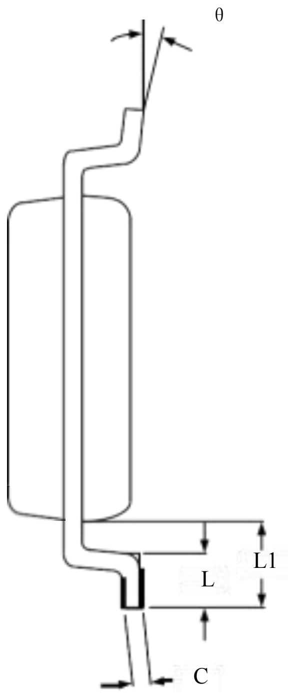
Dimensions

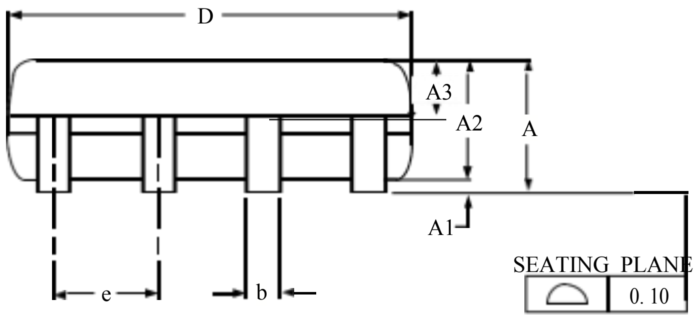
Symbol / Unit		A	A1	A2	A3	b	C	D	E	E1	e	L	L1	h	θ
mm	Min	-	0.10	1.30	0.6	0.39	0.20	4.80	5.80	3.80	1.27 BSC	0.50	1.05	0.25	0
	Nom	-	-	1.40	0.65	-	-	4.90	5.90	3.90		-		-	-
	Max	1.75	0.225	1.50	0.7	0.47	0.24	5.00	6.20	4.00		0.80		0.50	8
Inch	Min	-	0.004	0.051	0.024	0.015	0.008	0.189	0.228	0.150	0.050 BSC	0.020	0.041	0.010	0
	Nom	-	-	0.055	0.026	-	-	0.193	0.236	0.154		-		-	-
	Max	0.069	0.009	0.059	0.028	0.019	0.009	0.197	0.244	0.158		0.031		0.020	8

TITLE	DRAWING NO.	REV	REF
8-Lead SOP(150mil)		A	JEDEC MS-012

7.2-Lead SOP(208mil)





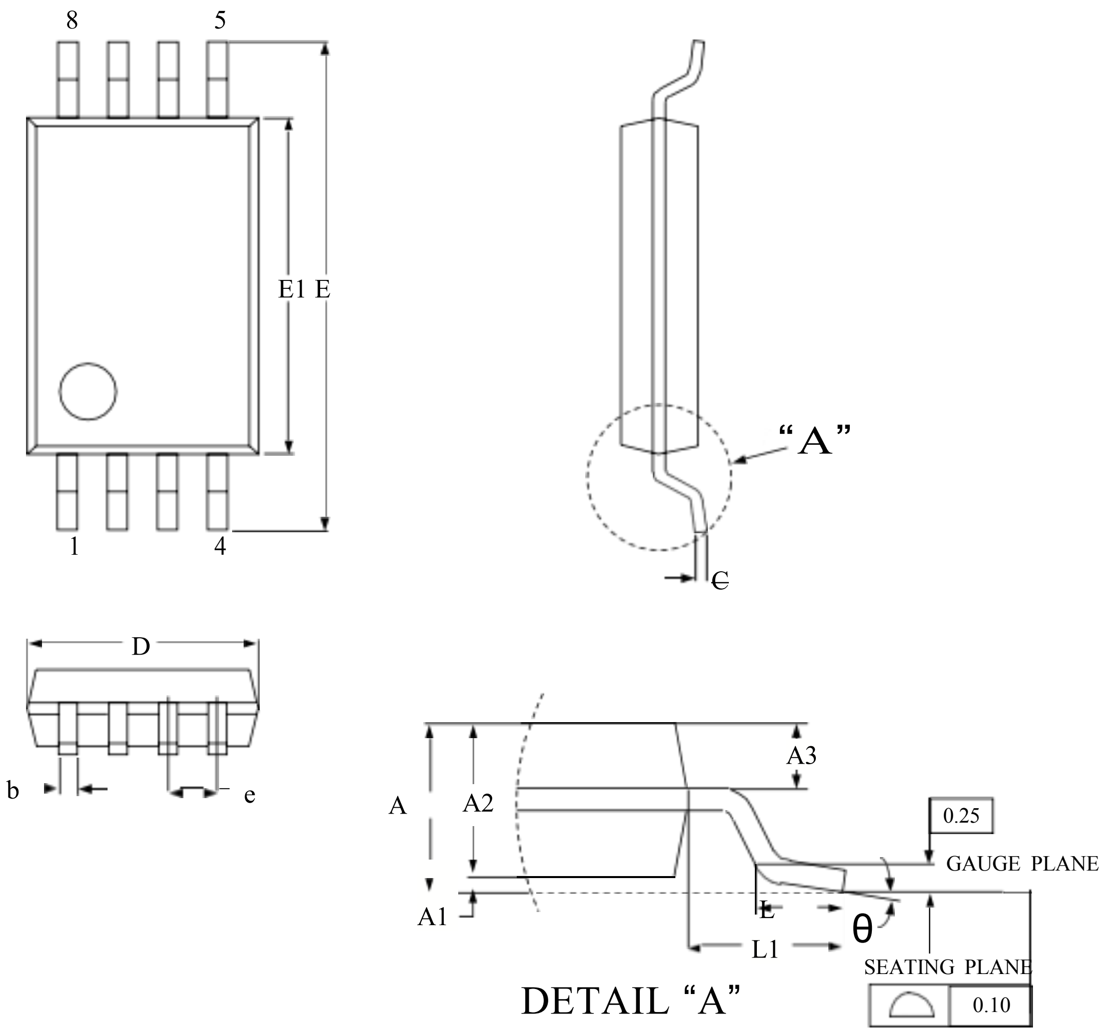


Dimensions

Symbol / Unit		A	A1	A2	A3	b	C	D	E	E1	e	L	L1	θ
mm	Min	1.75	0.05	1.70	0.55	0.38	0.203 REF	5.13	7.70	5.18	1.27 REF	0.50	1.21	0
	Nom	1.9	0.1	1.80	0.60	0.43		5.23	7.90	5.28		0.65	1.31	-
	Max	2.05	0.15	1.90	0.65	0.48		5.33	8.10	5.38		0.80	1.41	8
Inch	Min	0.069	0.002	0.067	0.022	0.015	0.008 REF	0.202	0.303	0.204	0.050 REF	0.020	0.048	0
	Nom	0.075	0.004	0.071	0.024	0.017		0.206	0.311	0.208		0.026	0.052	-
	Max	0.081	0.006	0.075	0.026	0.019		0.210	0.319	0.212		0.031	0.056	8

TITLE	DRAWING NO.	REV	REF
8-Lead SOP(208mil)		A	

7.3-Lead TSSOP(173mil)

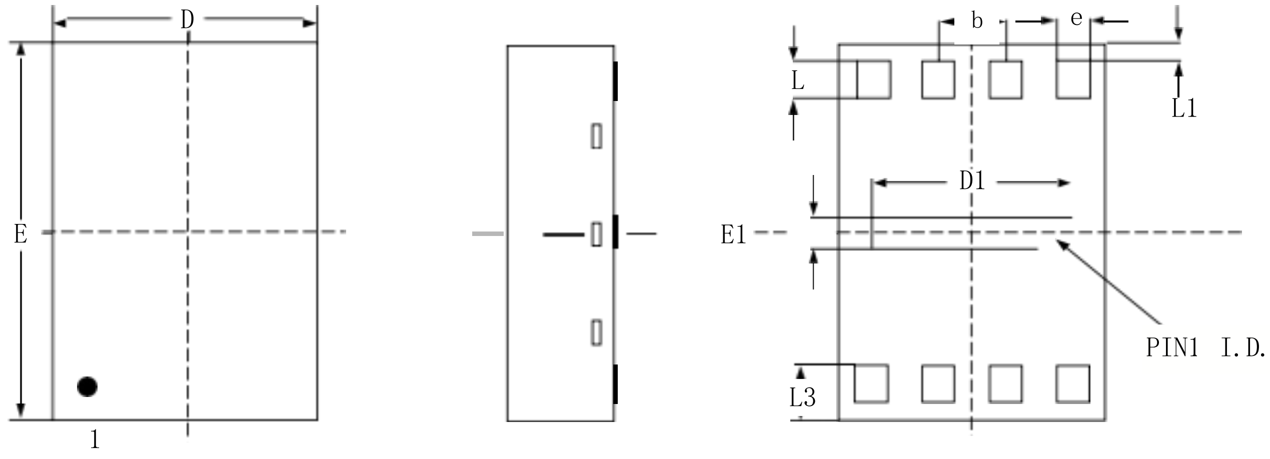


Dimensions

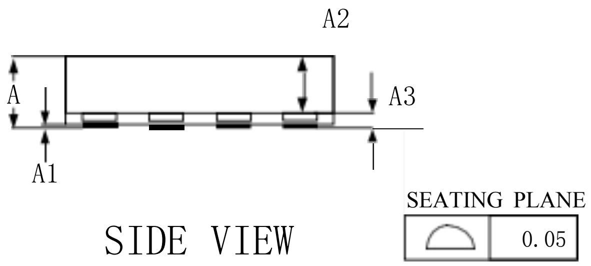
Symbol / Unit		A	A1	A2	A3	b	C	D	E	E1	e	L	L1	θ
mm	Min	-	0.05	0.90	0.39	0.20	0.13	2.90	6.20	4.30		0.45		0
	Nom	-	-	1.00	0.44	-	-	3.00	6.40	4.40	0.65 BSC	-	1.00 REF	-
	Max	1.20	0.15	1.05	0.49	0.28	0.17	3.10	6.60	4.50		0.75		8
Inch	Min	-	0.002	0.035	0.015	0.008	0.005	0.114	0.244	0.169		0.018		0
	Nom	-	-	0.039	0.017	-	-	0.118	0.252	0.173	0.026 BSC	-	0.039 REF	-
	Max	0.047	0.006	0.041	0.019	0.011	0.007	0.122	0.260	0.177		0.030		8

TITLE	DRAWING NO.	REV	REF
8-lead TSSOP		A	JEDEC MO-153

7.4-Land USON(3x2mm)



TOP VIEW BOTTOM VIEW



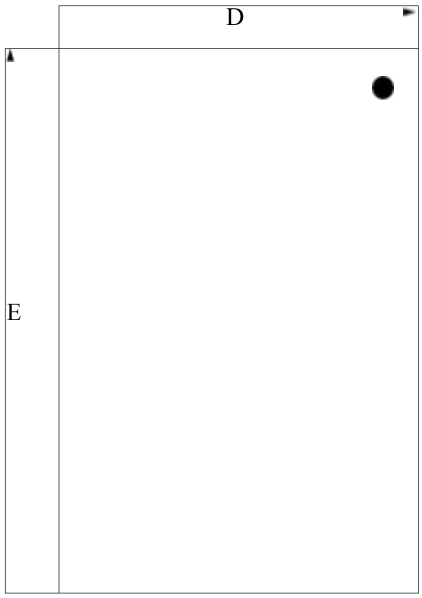
SIDE VIEW

Dimensions

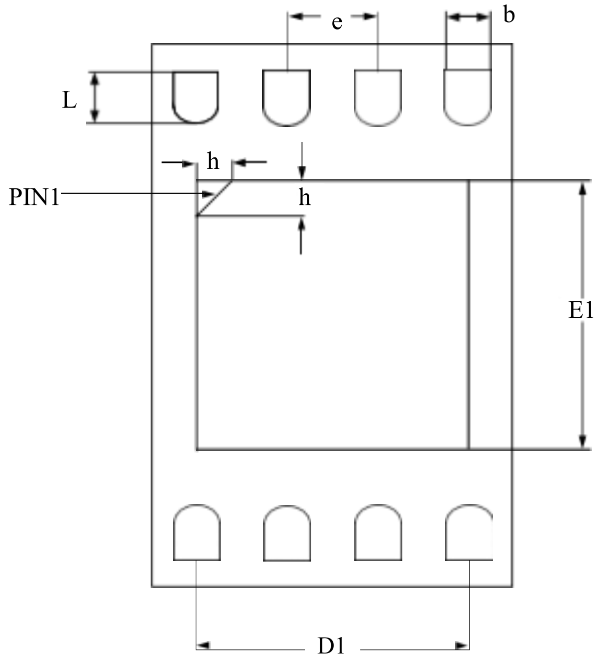
Symbol / Unit		A	A1	A2	A3	b	D	D1	E	E1	e	L	L1	L3
mm	Min	0.50	0.00	-	-	0.20	1.90	1.55	2.90	0.15		0.30	-	0.40
	Nom	0.55	0.02	0.40	0.15	0.25	2.00	1.60	3.00	0.20	0.50	0.35	0.10	0.45
	Max	0.60	0.05	-	-	0.30	2.10	1.65	3.10	0.25		0.40	-	0.50
Inch	Min	0.015	0.00	-	-	0.007	0.074	0.061	0.114	0.005		0.011	-	0.012
	Nom	0.018	---	0.012	0.005	0.010	0.079	0.063	0.118	0.008	0.02	0.013	0.004	0.016
	Max	0.019	0.001	-	-	0.012	0.082	0.064	0.122	0.009		0.015	-	0.020

TITLE	DRAWING NO.	REV	REF
DFN8L(0203X0 55-0 5)		A	JEDEC MO-252

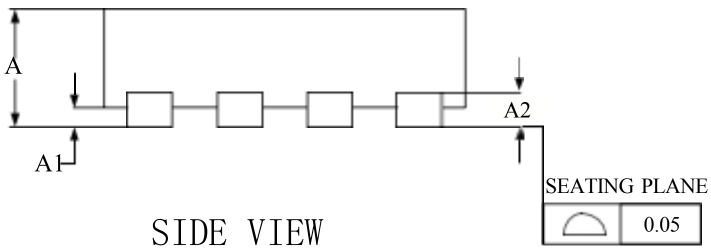
7.5-Land WSON(6x5mm)



TOP VIEW



BOTTOM VIEW



SIDE VIEW

Dimensions

Symbol / Unit		A	A1	A2	b	D	D1	E	E1	e	L	h
mm	Min	0.70	0.00	_	0.35	4.90	3.90	5.90	3.30	_	0.50	0.30
	Nom	0.75	0.02	0.203	0.40	5.00	4.00	6.00	3.40	1.27	0.60	0.35
	Max	0.80	0.05	_	0.48	5.10	4.10	6.10	3.50	_	0.75	0.40
Inch	Min	0.028	0.000	_	0.014	0.193	0.154	0.232	0.129	_	0.020	0.033
	Nom	0.030	_	0.008	0.016	0.197	0.157	0.236	0.134	0.05	0.024	0.039
	Max	0.032	0.002	_	0.019	0.201	0.161	0.240	0.138	_	0.030	0.045

TITLE	DRAWING NO.	REV	REF
DFN8 (0506X0 75- 1 27)		A	JEDEC MO-220

8. Revision History

Rev.	Date	Description
1.0	2019-10-11	Initial Release
1.1	2020-08-06	Modify Package Information